

SN8P2608

USER'S MANUAL

Version 1.5

SONiX 8-Bit Micro-Controller

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AMENDMENT HISTORY

| Version | Date | Description |
|-------------|------------|---|
| VER 0.1~0.3 | June. 2004 | V0.1 ~ V0.3 is short form only. |
| VER 0.4 | July. 2004 | Complete version first issue, |
| VER 0.5 | July. 2004 | 1. Change the description of "S" parameter in all instruction cycle related explanation. 2. Cancel the "B0MOV M, I" and "BOXCH A, M" instruction limitation. |
| VER 0.6 | July. 2004 | Remove all TC0 description and modify programming information. |
| VER 1.0 | Dec. 2004 | 1. Add T0, TC1, PWM application notices. 2. T0C doesn't support read and modify write instructions. 3. Modify operating mode, stack, reset, I/O, programming pins diagrams. 4. Modify timer, system clock descriptions. 5. Modify system clock description. 6. Remove ORG4~7 limitation. |
| VER 1.1 | Jan. 2005 | 1. Re-arrange partial edition layout. 2. Strongly recommend using SN8ICE-2K ICE to emulate SN8P2608. SN8IDE V1.99S or later No More support SN8P2000 series emulation. |
| | Nov.2005 | 1. ADD Brown-Out reset circuit. 2. ADD Working Voltage vs. Frequency graphs. |
| VER 1.2 | Dec 2005 | 1. Modify Topr value. 2. Modify Brown-Out Reset description 3. Remove power consumption(Pc) 4. Remove Noise Filter Enable Working Voltage 5. Modify M2IDE 1.07 6. Remove High clock32K mode 7. Modify ELECTRICAL CHARACTERISTIC. |
| VER 1.3 | Feb. 2007 | 1. Add Marking Definition. 2. Modify ELECTRICAL CHARACTERISTIC. 3. Modify RST/P4.7/VPP PIN DISCRIPTION. |
| VER 1.4 | Sep. 2007 | 1. Remove DIP48 package. |
| VER 1.5 | Oct. 2009 | Add LQFP48 package. |

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1 PRODUCT OVERVIEW

1.1 FEATURES

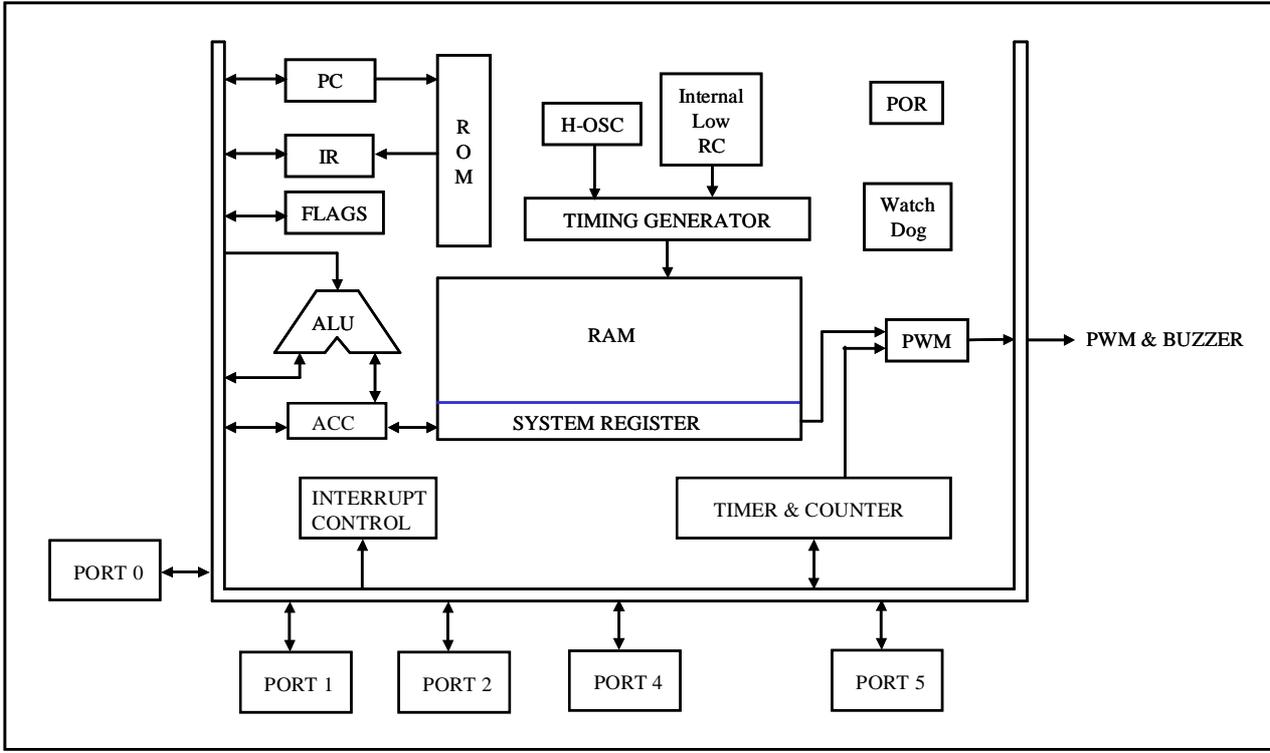
- ◆ **Memory configuration**
OTP ROM size: 6K * 16 bits.
RAM size: 128 * 8 bits.
Eight levels stack buffer
- ◆ **I/O pin configuration**
Bi-directional: P0, P1, P2, P4, P5
Input only: P4.7 shared with reset pin.
Programmable open-drain: P1.0, P1.1
Wakeup: P0, P1 level change trigger
Pull-up resistors: P0, P1, P2, P4, P5
External Interrupt trigger edge:
 P0.0 controlled by PEDGE register
 P0.1 is falling edge trigger only
- ◆ **Powerful instructions**
One clocks per instruction cycle (1T)
Most of instructions are one cycle only.
All ROM area JMP instruction.
All ROM area CALL address instruction.
All ROM area lookup table function (MOVC)
- ◆ **Four interrupt sources**
Two internal interrupts: T0, TC1.
Two external interrupts: INT0, INT1.
- ◆ **Two 8-bit Timer/Counter**
T0: Basic timer
TC1: Auto-reload timer/Counter/PWM1/Buzzer output
- ◆ **On chip watchdog timer and clock source is internal low clock RC type (16KHz @3V, 32KHz @5V).**
- ◆ **Dual system clocks**
External high clock: RC type up to 10 MHz
External high clock: Crystal type up to 16 MHz
Internal low clock: RC type 16KHz(3V), 32KHz(5V)
- ◆ **Operating modes**
Normal mode: Both high and low clock active
Slow mode: Low clock only
Sleep mode: Both high and low clock stop
Green mode: Periodical wakeup by T0 timer
- ◆ **Package (Chip form support)**
P-DIP 40 pins
SSOP 48 pins
LQFP 48 pins

F Features Selection Table

| CHIP | ROM | RAM | Stack | Timer | | I/O | Green Mode | PWM | Wakeup Pin No. | Package |
|----------|-------|-----|-------|-------|-----|-----|------------|--------|----------------|------------------|
| | | | | T0 | TC1 | | | Buzzer | | |
| SN8P2606 | 6K*16 | 128 | 8 | V | V | 34 | V | V | 16 | P-DIP 40 |
| SN8P2608 | 6K*16 | 128 | 8 | V | V | 40 | V | V | 16 | SSOP 48, LQFP 48 |

1.2 SYSTEM BLOCK DIAGRAM

SN8P2608/2606



1.3 PIN ASSIGNMENT

SN8P2606P (P-DIP 40 pins)

| | | | | |
|---------------|----|---|----|-----------|
| RST/VPP/P4.7 | 1 | U | 40 | P1.0 |
| P1.1 | 2 | | 39 | P0.7 |
| P1.2 | 3 | | 38 | P0.6 |
| P1.3 | 4 | | 37 | P0.5 |
| P1.4 | 5 | | 36 | P0.4 |
| P0.1/INT1 | 6 | | 35 | P0.3 |
| P1.5 | 7 | | 34 | P0.2 |
| P1.6 | 8 | | 33 | P0.0/INT0 |
| P1.7 | 9 | | 32 | VDD |
| P4.0 | 10 | | 31 | VSS |
| VDD | 11 | | 30 | P2.7 |
| VSS | 12 | | 29 | P2.6 |
| XIN | 13 | | 28 | P2.5 |
| XOUT/Fcpu | 14 | | 27 | P2.4 |
| P4.2 | 15 | | 26 | P2.3 |
| P5.5 | 16 | | 25 | P2.2 |
| P5.4 | 17 | | 24 | P2.1 |
| P5.3/PWM1/BZ1 | 18 | | 23 | P2.0 |
| P5.2 | 19 | | 22 | P5.6 |
| P5.1 | 20 | | 21 | P5.0 |

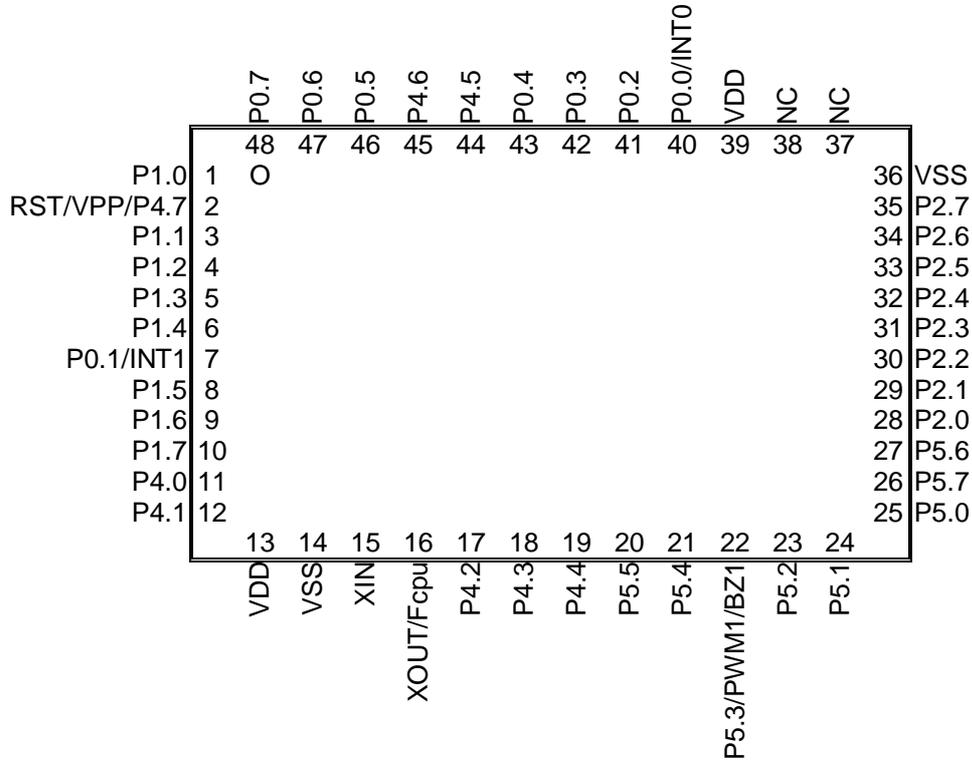
SN8P2606P

SN8P2608X (SSOP 48 pins)

| | | | | |
|---------------|----|---|----|-----------|
| P1.0 | 1 | U | 48 | P0.7 |
| RST/VPP/P4.7 | 2 | | 47 | P0.6 |
| P1.1 | 3 | | 46 | P0.5 |
| P1.2 | 4 | | 45 | P4.6 |
| P1.3 | 5 | | 44 | P4.5 |
| P1.4 | 6 | | 43 | P0.4 |
| P0.1/INT1 | 7 | | 42 | P0.3 |
| P1.5 | 8 | | 41 | P0.2 |
| P1.6 | 9 | | 40 | P0.0/INT0 |
| P1.7 | 10 | | 39 | VDD |
| P4.0 | 11 | | 38 | NC |
| P4.1 | 12 | | 37 | NC |
| VDD | 13 | | 36 | VSS |
| VSS | 14 | | 35 | P2.7 |
| XIN | 15 | | 34 | P2.6 |
| XOUT/Fcpu | 16 | | 33 | P2.5 |
| P4.2 | 17 | | 32 | P2.4 |
| P4.3 | 18 | | 31 | P2.3 |
| P4.4 | 19 | | 30 | P2.2 |
| P5.5 | 20 | | 29 | P2.1 |
| P5.4 | 21 | | 28 | P2.0 |
| P5.3/PWM1/BZ1 | 22 | | 27 | P5.6 |
| P5.2 | 23 | | 26 | P5.7 |
| P5.1 | 24 | | 25 | P5.0 |

SN8P2608X

SN8P2608Q (LQFP 48 pins)

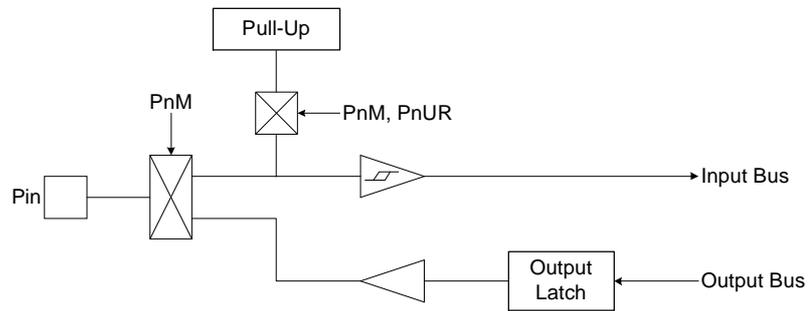


1.4 PIN DESCRIPTIONS

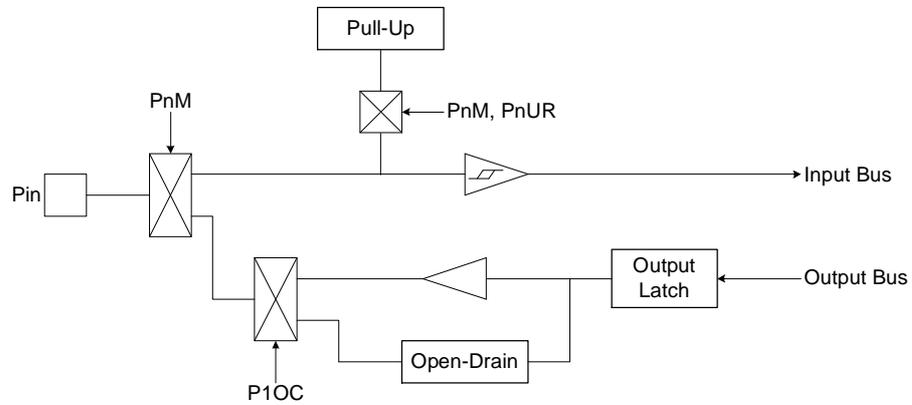
| PIN NAME | TYPE | DESCRIPTION |
|-------------------------|------|---|
| VDD, VSS | P | Power supply input pins for digital circuit. |
| P4.7/RST/VPP | I, P | P4.7: Input only pin (Schmitt trigger) if disable external reset function. P4.7 without build-in pull-up resistor. P4.7 is input only pin without pull-up resistor under P4.7 mode. Add the 100 ohm external resistor on P4.7, when it is set to be input pin. RST: System reset input pin. Schmitt trigger structure, low active, normal stay to "high". VPP: OTP programming pin. |
| XIN | I | Oscillator input pin while external oscillator enable (crystal and RC). |
| XOUT/Fcpu | I/O | XOUT: Oscillator output pin while external crystal enable. Fcpu: Signal output pin while external RC mode enable. |
| P0.0/INT0 | I/O | Port 0.0 bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. INT0 trigger pin (Schmitt trigger). |
| P0.1/INT1 | I/O | Port 0.1 bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. INT1 trigger pin (Schmitt trigger). TC1 event counter clock input pin. |
| P0.2~P0.7 | I/O | Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. |
| P1.0~P1.1 | I/O | Port 1.0, P1.1 bi-direction pin and open-drain pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. |
| P1.2~P1.7 | I/O | Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. |
| P2.0~P2.7 | I/O | Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. |
| P4.0~P4.6 | I/O | Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. |
| P5.0~P5.2, P5.4~P5.7 | I/O | Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. |
| P5.3/BZ1/PWM1 | I/O | Port 5.3 bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resistors. TC1 ÷ 2 signal output pin for buzzer or PWM1 output pin. |

1.5 PIN CIRCUIT DIAGRAMS

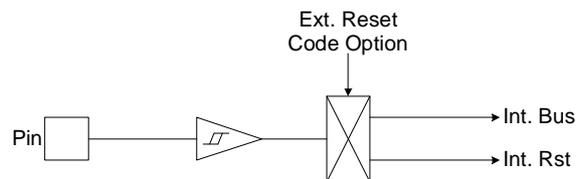
Port 0, 1, 2, 4, 5 structure:



Port 1.0, P1.1 structure:



Port 4.7 structure:

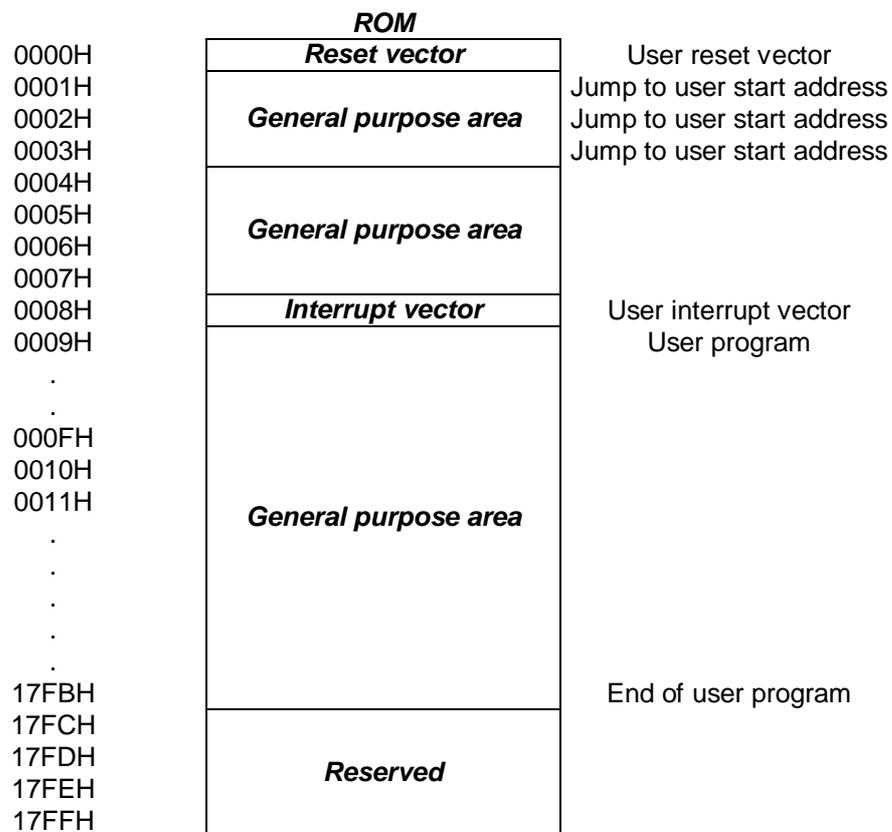


2 CENTRAL PROCESSOR UNIT (CPU)

2.1 MEMORY MAP

2.1.1 PROGRAM MEMORY (ROM)

F 6K words ROM



2.1.2 RESET VECTOR (0000H)

A one-word vector address area is used to execute system reset.

- F Power On Reset (NT0=1, NPD=0).
- F Watchdog Reset (NT0=0, NPD=0).
- F External Reset (NT0=1, NPD=1).

After power on reset, external reset or watchdog timer overflow reset, then the chip will restart the program from address 0000h and all system registers will be set as default values. It is easy to know reset status from NT0, NPD flags of PFLAG register. The following example shows the way to define the reset vector in the program memory.

Ø Example: Defining Reset Vector

```

                ORG      0          ; 0000H
                JMP      START     ; Jump to user program address.
                ...
START:         ORG      10H
                ; 0010H, The head of user program.
                ; User program
                ...
                ENDP           ; End of program

```

2.1.3 INTERRUPT VECTOR (0008H)

A 1-word vector address area is used to execute interrupt request. If any interrupt service executes, the program counter (PC) value is stored in stack buffer and jump to 0008h of program memory to execute the vectored interrupt. Users have to define the interrupt vector and the first instruction at ORG 8 must be "JMP" or "NOP". The following example shows the way to define the interrupt vector in the program memory.

- **Note: "PUSH", "POP" instructions save and load ACC/PFLAG without (NT0, NPD). PUSH/POP buffer is a unique buffer and only one level.**

- **Note: The first instruction at ORG 8 must be "JMP" or "NOP".**

Ø **Example: Defining Interrupt Vector. The interrupt service routine is following ORG 8.**

```
.CODE
    ORG      0          ; 0000H
    JMP     START      ; Jump to user program address.
    ...

    ORG      8          ; Interrupt vector.
    NOP                    ; The first instruction at ORG 8.
    PUSH                   ; Save ACC and PFLAG register to buffers.
    ...
    ...
    POP                    ; Load ACC and PFLAG register from buffers.
    RETI                  ; End of interrupt service routine
    ...

START:
    ...                  ; The head of user program.
    ...                  ; User program
    JMP     START        ; End of user program
    ...

    ENDP                ; End of program
```

Ø Example: Defining Interrupt Vector. The interrupt service routine is following user program.

```
.DATA      ACCBUF  DS  1      ; Define ACCBUF for store ACC data.
          PFLAGBUF DS  1      ; Define PFLAGBUF for store PFLAG data.
.CODE
          ORG     0          ; 0000H
          JMP     START      ; Jump to user program address.
          ...
          ORG     8          ; Interrupt vector.
          JMP     MY_IRQ    ; 0008H, Jump to interrupt service routine address.
          ...
START:    ORG     10H        ; 0010H, The head of user program.
          ...                ; User program.
          ...
          JMP     START      ; End of user program.
          ...
MY_IRQ:   ...                ; The head of interrupt service routine.
          PUSH    ; Save ACC and PFLAG register to buffers.
          ...
          ...
          POP     ; Load ACC and PFLAG register from buffers.
          RETI   ; End of interrupt service routine.
          ...
          ENDP              ; End of program.
```

- *Note: It is easy to understand the rules of SONiX program from demo programs given above. These points are as following:*

1. *The address 0000H is a "JMP" instruction to make the program starts from the beginning.*
2. *The address 0008H is interrupt vector and the first instruction must be "NOP" or "JMP".*
3. *User's program is a loop routine for main purpose application.*

2.1.4 LOOK-UP TABLE DESCRIPTION

In the ROM's data lookup function, Y register is pointed to middle byte address (bit 8~bit 15) and Z register is pointed to low byte address (bit 0~bit 7) of ROM. After MOVC instruction executed, the low-byte data will be stored in ACC and high-byte data stored in R register.

Ø **Example: To look up the ROM data located "TABLE1".**

```

        B0MOV    Y, #TABLE1$M    ; To set lookup table1's middle address
        B0MOV    Z, #TABLE1$L    ; To set lookup table1's low address.
        MOVC     ; To lookup data, R = 00H, ACC = 35H

                                ; Increment the index address for next address.
        INCMS    Z                ; Z+1
        JMP     @F                ; Z is not overflow.
        INCMS    Y                ; Z overflow (FFH à 00), à Y=Y+1
        NOP

@@:    MOVC     ; To lookup data, R = 51H, ACC = 05H.
        ...
TABLE1: DW     0035H            ; To define a word (16 bits) data.
        DW     5105H
        DW     2012H
        ...

```

- **Note: The Y register will not increase automatically when Z register crosses boundary from 0xFF to 0x00. Therefore, user must take care such situation to avoid look-up table errors. If Z register is overflow, Y register must be added one. The following INC_YZ macro shows a simple method to process Y and Z registers automatically.**

Ø **Example: INC_YZ macro.**

```

INC_YZ    MACRO
        INCMS    Z                ; Z+1
        JMP     @F                ; Not overflow

        INCMS    Y                ; Y+1
        NOP     ; Not overflow

@@:
        ENDM

```

Ø Example: Modify above example by "INC_YZ" macro.

```

B0MOV    Y, #TABLE1$M    ; To set lookup table1's middle address
B0MOV    Z, #TABLE1$L    ; To set lookup table1's low address.
MOVC                                          ; To lookup data, R = 00H, ACC = 35H

    INC_YZ                ; Increment the index address for next address.
    ;
@@:      MOVC              ; To lookup data, R = 51H, ACC = 05H.
    ;
TABLE1:  DW                ; To define a word (16 bits) data.
    DW    0035H
    DW    5105H
    DW    2012H
    ;

```

The other example of look-up table is to add Y or Z index register by accumulator. Please be careful if "carry" happen.

Ø Example: Increase Y and Z register by B0ADD/ADD instruction.

```

B0MOV    Y, #TABLE1$M    ; To set lookup table's middle address.
B0MOV    Z, #TABLE1$L    ; To set lookup table's low address.

    B0MOV    A, BUF        ; Z = Z + BUF.
    B0ADD    Z, A

    B0BTS1   FC            ; Check the carry flag.
    JMP     GETDATA        ; FC = 0
    INCMS   Y              ; FC = 1. Y+1.
    NOP

GETDATA:                                          ;
    MOVC                                          ; To lookup data. If BUF = 0, data is 0x0035
    ; If BUF = 1, data is 0x5105
    ; If BUF = 2, data is 0x2012
    ;
    ;
TABLE1:  DW                ; To define a word (16 bits) data.
    DW    0035H
    DW    5105H
    DW    2012H
    ;

```

2.1.5 JUMP TABLE DESCRIPTION

The jump table operation is one of multi-address jumping function. Add low-byte program counter (PCL) and ACC value to get one new PCL. If PCL is overflow after PCL+ACC, PCH adds one automatically. The new program counter (PC) points to a series jump instructions as a listing table. It is easy to make a multi-jump program depends on the value of the accumulator (A).

- **Note: PCH only support PC up counting result and doesn't support PC down counting. When PCL is carry after PCL+ACC, PCH adds one automatically. If PCL borrow after PCL-ACC, PCH keeps value and not change.**

Ø Example: Jump table.

```

ORG      0X0100      ; The jump table is from the head of the ROM boundary

B0ADD    PCL, A      ; PCL = PCL + ACC, PCH + 1 when PCL overflow occurs.
JMP      A0POINT    ; ACC = 0, jump to A0POINT
JMP      A1POINT    ; ACC = 1, jump to A1POINT
JMP      A2POINT    ; ACC = 2, jump to A2POINT
JMP      A3POINT    ; ACC = 3, jump to A3POINT

```

SONiX provides a macro for safe jump table function. This macro will check the ROM boundary and move the jump table to the right position automatically. The side effect of this macro maybe wastes some ROM size.

Ø Example: If “jump table” crosses over ROM boundary will cause errors.

```

@JMP_A    MACRO      VAL
IF        (($+1) !& 0XFF00) != (($+(VAL)) !& 0XFF00)
JMP      ($ | 0XFF)
ORG      ($ | 0XFF)
ENDIF
ADD      PCL, A
ENDM

```

- **Note: “VAL” is the number of the jump table listing number.**

Ø Example: “@JMP_A” application in SONiX macro file called “MACRO3.H”.

```

B0MOV    A, BUF0      ; "BUF0" is from 0 to 4.
@JMP_A   5            ; The number of the jump table listing is five.
JMP      A0POINT     ; ACC = 0, jump to A0POINT
JMP      A1POINT     ; ACC = 1, jump to A1POINT
JMP      A2POINT     ; ACC = 2, jump to A2POINT
JMP      A3POINT     ; ACC = 3, jump to A3POINT
JMP      A4POINT     ; ACC = 4, jump to A4POINT

```

If the jump table position is across a ROM boundary (0x00FF~0x0100), the “@JMP_A” macro will adjust the jump table routine begin from next RAM boundary (0x0100).

Ø Example: “@JMP_A” operation.

; Before compiling program.

```

ROM address
          B0MOV    A, BUF0      ; "BUF0" is from 0 to 4.
          @JMP_A   5            ; The number of the jump table listing is five.
0X00FD   JMP      A0POINT     ; ACC = 0, jump to A0POINT
0X00FE   JMP      A1POINT     ; ACC = 1, jump to A1POINT
0X00FF   JMP      A2POINT     ; ACC = 2, jump to A2POINT
0X0100   JMP      A3POINT     ; ACC = 3, jump to A3POINT
0X0101   JMP      A4POINT     ; ACC = 4, jump to A4POINT

```

; After compiling program.

```

ROM address
          B0MOV    A, BUF0      ; "BUF0" is from 0 to 4.
          @JMP_A   5            ; The number of the jump table listing is five.
0X0100   JMP      A0POINT     ; ACC = 0, jump to A0POINT
0X0101   JMP      A1POINT     ; ACC = 1, jump to A1POINT
0X0102   JMP      A2POINT     ; ACC = 2, jump to A2POINT
0X0103   JMP      A3POINT     ; ACC = 3, jump to A3POINT
0X0104   JMP      A4POINT     ; ACC = 4, jump to A4POINT

```

2.1.6 CHECKSUM CALCULATION

The last ROM address are reserved area. User should avoid these addresses (last address) when calculate the Checksum value.

Ø **Example: The demo program shows how to calculated Checksum from 00H to the end of user's code.**

```

MOV      A,#END_USER_CODE$L
B0MOV   END_ADDR1, A      ; Save low end address to end_addr1
MOV      A,#END_USER_CODE$M
B0MOV   END_ADDR2, A      ; Save middle end address to end_addr2
CLR      Y                ; Set Y to 00H
CLR      Z                ; Set Z to 00H

@@:
MOV      FC
B0BSET  FC                ; Clear C flag
ADD      DATA1, A        ; Add A to Data1
MOV      A, R
ADC      DATA2, A        ; Add R to Data2
JMP      END_CHECK        ; Check if the YZ address = the end of code

AAA:
INCMS   Z                ; Z=Z+1
JMP     @B                ; If Z != 00H calculate to next address
JMP     Y_ADD_1          ; If Z = 00H increase Y

END_CHECK:
MOV      A, END_ADDR1
CMPRS   A, Z              ; Check if Z = low end address
JMP     AAA              ; If Not jump to checksum calculate
MOV      A, END_ADDR2
CMPRS   A, Y              ; If Yes, check if Y = middle end address
JMP     AAA              ; If Not jump to checksum calculate
JMP     CHECKSUM_END     ; If Yes checksum calculated is done.

Y_ADD_1:
INCMS   Y                ; Increase Y
NOP
JMP     @B                ; Jump to checksum calculate

CHECKSUM_END:
...
...

END_USER_CODE:          ; Label of program end

```

2.1.7 CODE OPTION TABLE

| Code Option | Content | Function Description |
|--------------|-----------|--|
| High_Clk | RC | Low cost RC for external high clock oscillator and XOUT becomes to Fcpu output pin. |
| | 12M X'tal | High speed crystal /resonator (e.g. 12MHz) for external high clock oscillator. |
| | 4M X'tal | Standard crystal /resonator (e.g. 4M) for external high clock oscillator. |
| Watch_Dog | Always_On | Watchdog timer always on even in power down and green mode. |
| | Enable | Enable watchdog timer. Watchdog timer stops in power down mode and green mode. |
| | Disable | Disable Watchdog function. |
| Fcpu | Fosc/1 | Instruction cycle is oscillator clock. Notice: In Fosc/1, Noise Filter must be disabled. |
| | Fosc/2 | Instruction cycle is 2 oscillator clocks. Notice: In Fosc/2, Noise Filter must be disabled. |
| | Fosc/4 | Instruction cycle is 4 oscillator clocks. |
| | Fosc/8 | Instruction cycle is 8 oscillator clocks. |
| Reset_Pin | Reset | Enable External reset pin. |
| | P47 | Enable P4.7 input only without pull-up resistor. |
| Security | Enable | Enable ROM code Security function. |
| | Disable | Disable ROM code Security function. |
| Noise_Filter | Enable | Enable Noise Filter and the Fcpu is Fosc/4~Fosc/8. |
| | Disable | Disable Noise Filter and the Fcpu is Fosc/1~Fosc/8. |

- **Note:**

1. In high noisy environment, enable "Noise Filter" and set Watch_Dog as "Always_On" is strongly recommended. Enable "Noise_Filter" will limit the Fcpu = Fosc/4 ~ Fosc/8.
2. If users define watchdog as "Always_On", assembler will Enable "Watch_Dog" automatically.
3. Fcpu code option is only available for High Clock. Fcpu of slow mode is Fosc/4 (the Fosc is internal low clock).

2.1.8 DATA MEMORY (RAM)

F 128 X 8-bit RAM

| | | RAM location | |
|---------------|---------------------------|-----------------------------|---|
| BANK 0 | Address | | |
| | 000h | General purpose area | |
| | " | | |
| | " | | |
| | " | | |
| | " | | |
| | 07Fh | System register | |
| | 080h | | 080h~0FFh of Bank 0 store system registers (128 bytes). |
| | " | | |
| | " | | |
| | " | | |
| 0FFh | End of bank 0 area | | |

2.1.9 SYSTEM REGISTER

2.1.9.1 SYSTEM REGISTER TABLE

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 8 | L | H | R | Z | Y | - | PFLAG | - | - | - | - | - | - | - | - | - |
| 9 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B | - | - | - | - | - | - | - | - | P0M | - | - | - | - | - | - | PEDGE |
| C | P1W | P1M | P2M | - | P4M | P5M | - | - | INTRQ | INTEN | OSCM | - | WDTR | - | PCL | PCH |
| D | P0 | P1 | P2 | - | P4 | P5 | - | - | T0M | T0C | - | - | TC1M | TC1C | TC1R | STKP |
| E | P0UR | P1UR | P2UR | - | P4UR | P5UR | @HL | @YZ | - | P1OC | - | - | - | - | - | - |
| F | STK7L | STK7H | STK6L | STK6H | STK5L | STK5H | STK4L | STK4H | STK3L | STK3H | STK2L | STK2H | STK1L | STK1H | STK0L | STK0H |

Description

PFLAG = ROM page and special flag register.

H, L = Working, @HL and ROM addressing register.

P1W = Port 1 wakeup register.

PnM = Port n input/output mode register.

P1OC = Port 1 open-drain control register.

INTRQ = Interrupt request register.

OSCM = Oscillator mode register.

T0M = T0 mode register.

TC1M = TC1 mode register.

TC1R = TC1 auto-reload data buffer.

STKP = Stack pointer buffer.

@YZ = RAM YZ indirect addressing index pointer.

R = Working register and ROM look-up data buffer.

Y, Z = Working, @YZ and ROM addressing register.

PEDGE = P0.0 edge direction register.

Pn = Port n data buffer.

PnUR = Port n pull-up resistor control register.

INTEN = Interrupt enable register.

PCH, PCL = Program counter.

T0C = T0 counting register.

TC1C = TC1 counting register.

WDTR = Watchdog timer clear register.

STK0-STK7 = Stack 0 ~ stack 7 buffer.

@HL = RAM HL indirect addressing index pointer.

2.1.9.2 BIT DEFINITION of SYSTEM REGISTER

| Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | R/W | Remarks |
|---------|--------|----------|----------|----------|--------|--------|--------|---------|-----|---------|
| 080H | LBIT7 | LBIT6 | LBIT5 | LBIT4 | LBIT3 | LBIT2 | LBIT1 | LBIT0 | R/W | L |
| 081H | HBIT7 | HBIT6 | HBIT5 | HBIT4 | HBIT3 | HBIT2 | HBIT1 | HBIT0 | R/W | H |
| 082H | RBIT7 | RBIT6 | RBIT5 | RBIT4 | RBIT3 | RBIT2 | RBIT1 | RBIT0 | R/W | R |
| 083H | ZBIT7 | ZBIT6 | ZBIT5 | ZBIT4 | ZBIT3 | ZBIT2 | ZBIT1 | ZBIT0 | R/W | Z |
| 084H | YBIT7 | YBIT6 | YBIT5 | YBIT4 | YBIT3 | YBIT2 | YBIT1 | YBIT0 | R/W | Y |
| 086H | NT0 | NPD | | | | C | DC | Z | R/W | PFLAG |
| 0B8H | P07M | P06M | P05M | P04M | P03M | P02M | P01M | P00M | R/W | P0M |
| 0BFH | | | | P00G1 | P00G0 | | | | R/W | PEDGE |
| 0C0H | P17W | P16W | P15W | P14W | P13W | P12W | P11W | P10W | W | P1W |
| 0C1H | P17M | P16M | P15M | P14M | P13M | P12M | P11M | P10M | R/W | P1M |
| 0C2H | P27M | P26M | P25M | P24M | P23M | P22M | P21M | P20M | R/W | P2M |
| 0C4H | | P46M | P45M | P44M | P43M | P42M | P41M | P40M | R/W | P4M |
| 0C5H | P57M | P56M | P55M | P54M | P53M | P52M | P51M | P50M | R/W | P5M |
| 0C8H | | TC1IRQ | | T0IRQ | | | P01IRQ | P00IRQ | R/W | INTRQ |
| 0C9H | | TC1IEN | | T0IEN | | | P01IEN | P00IEN | R/W | INTEN |
| 0CAH | | | | CPUM1 | CPUM0 | CLKMD | STPHX | | R/W | OSCM |
| 0CCH | WDTR7 | WDTR6 | WDTR5 | WDTR4 | WDTR3 | WDTR2 | WDTR1 | WDTR0 | W | WDTR |
| 0CEH | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 | R/W | PCL |
| 0CFH | | | | PC12 | PC11 | PC10 | PC9 | PC8 | R/W | PCH |
| 0D0H | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 | R/W | P0 |
| 0D1H | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | R/W | P1 |
| 0D2H | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | R/W | P2 |
| 0D4H | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 | R/W | P4 |
| 0D5H | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 | R/W | P5 |
| 0D8H | T0ENB | T0rate2 | T0rate1 | T0rate0 | | | | | R/W | T0M |
| 0D9H | T0C7 | T0C6 | T0C5 | T0C4 | T0C3 | T0C2 | T0C1 | T0C0 | R/W | T0C |
| 0DCH | TC1ENB | TC1rate2 | TC1rate1 | TC1rate0 | TC1CKS | ALOAD1 | TC1OUT | PWM1OUT | R/W | TC1M |
| 0DDH | TC1C7 | TC1C6 | TC1C5 | TC1C4 | TC1C3 | TC1C2 | TC1C1 | TC1C0 | R/W | TC1C |
| 0DEH | TC1R7 | TC1R6 | TC1R5 | TC1R4 | TC1R3 | TC1R2 | TC1R1 | TC1R0 | W | TC1R |
| 0DFH | GIE | | | | | STKPB2 | STKPB1 | STKPB0 | R/W | STKP |
| 0E0H | P07R | P06R | P05R | P04R | P03R | P02R | P01R | P00R | W | P0UR |
| 0E1H | P17R | P16R | P15R | P14R | P13R | P12R | P11R | P10R | W | P1UR |
| 0E2H | P27R | P26R | P25R | P24R | P23R | P22R | P21R | P20R | W | P2UR |
| 0E4H | | P46R | P45R | P44R | P43R | P42R | P41R | P40R | W | P4UR |
| 0E5H | P57R | P56R | P55R | P54R | P53R | P52R | P51R | P50R | W | P5UR |
| 0E6H | @HL7 | @ HL 6 | @ HL5 | @ HL4 | @ HL3 | @ HL2 | @ HL1 | @ HL0 | R/W | @ HL |
| 0E7H | @YZ7 | @YZ6 | @YZ5 | @YZ4 | @YZ3 | @YZ2 | @YZ1 | @YZ0 | R/W | @YZ |
| 0E9H | | | | | | | P11OC | P10OC | W | P1OC |
| 0F0H | S7PC7 | S7PC6 | S7PC5 | S7PC4 | S7PC3 | S7PC2 | S7PC1 | S7PC0 | R/W | STK7L |
| 0F1H | - | - | - | S7PC12 | S7PC11 | S7PC10 | S7PC9 | S7PC8 | R/W | STK7H |
| 0F2H | S6PC7 | S6PC6 | S6PC5 | S6PC4 | S6PC3 | S6PC2 | S6PC1 | S6PC0 | R/W | STK6L |
| 0F3H | - | - | - | S6PC12 | S6PC11 | S6PC10 | S6PC9 | S6PC8 | R/W | STK6H |
| 0F4H | S5PC7 | S5PC6 | S5PC5 | S5PC4 | S5PC3 | S5PC2 | S5PC1 | S5PC0 | R/W | STK5L |
| 0F5H | - | - | - | S6PC12 | S5PC11 | S5PC10 | S5PC9 | S5PC8 | R/W | STK5H |
| 0F6H | S4PC7 | S4PC6 | S4PC5 | S4PC4 | S4PC3 | S4PC2 | S4PC1 | S4PC0 | R/W | STK4L |
| 0F7H | - | - | - | S4PC12 | S4PC11 | S4PC10 | S4PC9 | S4PC8 | R/W | STK4H |
| 0F8H | S3PC7 | S3PC6 | S3PC5 | S3PC4 | S3PC3 | S3PC2 | S3PC1 | S3PC0 | R/W | STK3L |
| 0F9H | | | | S3PC12 | S3PC11 | S3PC10 | S3PC9 | S3PC8 | R/W | STK3H |
| 0FAH | S2PC7 | S2PC6 | S2PC5 | S2PC4 | S2PC3 | S2PC2 | S2PC1 | S2PC0 | R/W | STK2L |
| 0FBH | | | | S2PC12 | S2PC11 | S2PC10 | S2PC9 | S2PC8 | R/W | STK2H |
| 0FCH | S1PC7 | S1PC6 | S1PC5 | S1PC4 | S1PC3 | S1PC2 | S1PC1 | S1PC0 | R/W | STK1L |
| 0FDH | | | | S1PC12 | S1PC11 | S1PC10 | S1PC9 | S1PC8 | R/W | STK1H |
| 0FEH | S0PC7 | S0PC6 | S0PC5 | S0PC4 | S0PC3 | S0PC2 | S0PC1 | S0PC0 | R/W | STK0L |
| 0FFH | | | | S0PC12 | S0PC11 | S0PC10 | S0PC9 | S0PC8 | R/W | STK0H |

Note:

1. To avoid system error, make sure to put all the "0" and "1" as it indicates in the above table.
2. All of register names had been declared in SN8ASM assembler.
3. One-bit name had been declared in SN8ASM assembler with "F" prefix code.
4. "b0bset", "b0bclr", "bset", "bclr" instructions are only available to the "R/W" registers.
5. For detail description, please refer to the "System Register Quick Reference Table".

2.1.10 ACCUMULATOR

The ACC is an 8-bit data register responsible for transferring or manipulating data between ALU and data memory. If the result of operating is zero (Z) or there is carry (C or DC) occurrence, then these flags will be set to PFLAG register. ACC is not in data memory (RAM), so ACC can't be access by "B0MOV" instruction during the instant addressing mode.

Ø Example: Read and write ACC value.

; Read ACC data and store in BUF data memory.

```
MOV     BUF, A
```

; Write a immediate data into ACC.

```
MOV     A, #0FH
```

; Write ACC data from BUF data memory.

```
MOV     A, BUF
```

; or

```
B0MOV   A, BUF
```

The system doesn't store ACC and PFLAG value when interrupt executed. ACC and PFLAG data must be saved to other data memories. "PUSH", "POP" save and load ACC, PFLAG data into buffers.

Ø Example: Protect ACC and working registers.

INT_SERVICE:

```
PUSH     ; Save ACC and PFLAG to buffers.
```

```
...
```

```
POP     ; Load ACC and PFLAG from buffers.
```

```
RETI    ; Exit interrupt service vector
```

2.1.11 PROGRAM FLAG

The PFLAG register contains the arithmetic status of ALU operation, system reset status and LVD detecting status. NT0, NPD bits indicate system reset status including power on reset, LVD reset, reset by external pin active and watchdog reset. C, DC, Z bits indicate the result status of ALU operation.

| 086H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| PFLAG | NT0 | NPD | - | - | - | C | DC | Z |
| Read/Write | R/W | R/W | - | - | - | R/W | R/W | R/W |
| After reset | - | - | - | - | - | 0 | 0 | 0 |

Bit [7:6] **NT0, NPD**: Reset status flag.

| NT0 | NPD | Reset Status |
|-----|-----|-----------------------------|
| 0 | 0 | Watch-dog time out |
| 0 | 1 | Reserved |
| 1 | 0 | Reset by LVD |
| 1 | 1 | Reset by external Reset Pin |

Bit 2 **C**: Carry flag
 1 = Addition with carry, subtraction without borrowing, rotation with shifting out logic "1", comparison result ≥ 0 .
 0 = Addition without carry, subtraction with borrowing signal, rotation with shifting out logic "0", comparison result < 0 .

Bit 1 **DC**: Decimal carry flag
 1 = Addition with carry from low nibble, subtraction without borrow from high nibble.
 0 = Addition without carry from low nibble, subtraction with borrow from high nibble.

Bit 0 **Z**: Zero flag
 1 = The result of an arithmetic/logic/branch operation is zero.
 0 = The result of an arithmetic/logic/branch operation is not zero.

- **Note: Refer to instruction set table for detailed information of C, DC and Z flags.**

2.1.12 PROGRAM COUNTER

The program counter (PC) is a 13-bit binary counter separated into the high-byte 5 and the low-byte 8 bits. This counter is responsible for pointing a location in order to fetch an instruction for kernel circuit. Normally, the program counter is automatically incremented with each instruction during program execution.

Besides, it can be replaced with specific address by executing CALL or JMP instruction. When JMP or CALL instruction is executed, the destination address will be inserted to bit 0 ~ bit 12.

| | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| PC | - | - | - | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| After reset | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | PCH | | | | | | | | PCL | | | | | | | |

F ONE ADDRESS SKIPPING

There are nine instructions (CMPRS, INCS, INCMS, DECS, DECMS, BTS0, BTS1, B0BTS0, B0BTS1) with one address skipping function. If the result of these instructions is true, the PC will add 2 steps to skip next instruction.

If the condition of bit test instruction is true, the PC will add 2 steps to skip next instruction.

```

        B0BTS1    FC           ; To skip, if Carry_flag = 1
        JMP      C0STEP      ; Else jump to C0STEP.
        ...
        ...
C0STEP:    NOP

        B0MOV    A, BUF0     ; Move BUF0 value to ACC.
        B0BTS0    FZ           ; To skip, if Zero flag = 0.
        JMP      C1STEP      ; Else jump to C1STEP.
        ...
        ...
C1STEP:    NOP
    
```

If the ACC is equal to the immediate data or memory, the PC will add 2 steps to skip next instruction.

```

        CMPRS    A, #12H     ; To skip, if ACC = 12H.
        JMP      C0STEP      ; Else jump to C0STEP.
        ...
        ...
C0STEP:    NOP
    
```

If the destination increased by 1, which results overflow of 0xFF to 0x00, the PC will add 2 steps to skip next instruction.

INCS instruction:

INCS BUF0
JMP C0STEP ; Jump to C0STEP if ACC is not zero.

...

...

C0STEP: NOP

INCMS instruction:

INCMS BUF0
JMP C0STEP ; Jump to C0STEP if BUF0 is not zero.

...

...

C0STEP: NOP

If the destination decreased by 1, which results underflow of 0x00 to 0xFF, the PC will add 2 steps to skip next instruction.

DECS instruction:

DECS BUF0
JMP C0STEP ; Jump to C0STEP if ACC is not zero.

...

...

C0STEP: NOP

DECMS instruction:

DECMS BUF0
JMP C0STEP ; Jump to C0STEP if BUF0 is not zero.

...

...

C0STEP: NOP

F MULTI-ADDRESS JUMPING

Users can jump around the multi-address by either JMP instruction or ADD M, A instruction (M = PCL) to activate multi-address jumping function. Program Counter supports “ADD M,A”, ”ADC M,A” and “B0ADD M,A” instructions for carry to PCH when PCL overflow automatically. For jump table or others applications, users can calculate PC value by the three instructions and don't care PCL overflow problem.

- **Note: PCH only support PC up counting result and doesn't support PC down counting. When PCL is carry after PCL+ACC, PCH adds one automatically. If PCL borrow after PCL-ACC, PCH keeps value and not change.**

Ø **Example: If PC = 0323H (PCH = 03H, PCL = 23H)**

```
; PC = 0323H
      MOV      A, #28H
      B0MOV    PCL, A           ; Jump to address 0328H
      ...

; PC = 0328H
      MOV      A, #00H
      B0MOV    PCL, A           ; Jump to address 0300H
      ...
```

Ø **Example: If PC = 0323H (PCH = 03H, PCL = 23H)**

```
; PC = 0323H
      B0ADD    PCL, A           ; PCL = PCL + ACC, the PCH cannot be changed.
      JMP      A0POINT         ; If ACC = 0, jump to A0POINT
      JMP      A1POINT         ; ACC = 1, jump to A1POINT
      JMP      A2POINT         ; ACC = 2, jump to A2POINT
      JMP      A3POINT         ; ACC = 3, jump to A3POINT
      ...
      ...
```

2.1.13 H, L REGISTERS

The H and L registers are the 8-bit buffers. There are two major functions of these registers.

- I can be used as general working registers
- I can be used as RAM data pointers with @HL register

| 081H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| H | HBIT7 | HBIT6 | HBIT5 | HBIT4 | HBIT3 | HBIT2 | HBIT1 | HBIT0 |
| Read/Write | R/W |
| After reset | X | X | X | X | X | X | X | X |

| 080H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| L | LBIT7 | LBIT6 | LBIT5 | LBIT4 | LBIT3 | LBIT2 | LBIT1 | LBIT0 |
| Read/Write | R/W |
| After reset | X | X | X | X | X | X | X | X |

Example: If want to read a data from RAM address 20H of bank_0, it can use indirectly addressing mode to access data as following.

```

B0MOV    H, #00H        ; To set RAM bank 0 for H register
B0MOV    L, #20H        ; To set location 20H for L register
B0MOV    A, @HL         ; To read a data into ACC
    
```

Example: Clear general-purpose data memory area of bank 0 using @HL register.

```

CLR      H              ; H = 0, bank 0
B0MOV    L, #07FH       ; L = 7FH, the last address of the data memory area

CLR_HL_BUF:
CLR      @HL            ; Clear @HL to be zero
DECMS    L              ; L - 1, if L = 0, finish the routine
JMP      CLR_HL_BUF     ; Not zero

END_CLR:
CLR      @HL            ; End of clear general purpose data memory area of bank 0
...
    
```

2.1.14 Y, Z REGISTERS

The Y and Z registers are the 8-bit buffers. There are three major functions of these registers.

- | can be used as general working registers
- | can be used as RAM data pointers with @YZ register
- | can be used as ROM data pointer with the MOVC instruction for look-up table

| 084H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Y | YBIT7 | YBIT6 | YBIT5 | YBIT4 | YBIT3 | YBIT2 | YBIT1 | YBIT0 |
| Read/Write | R/W |
| After reset | - | - | - | - | - | - | - | - |

| 083H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Z | ZBIT7 | ZBIT6 | ZBIT5 | ZBIT4 | ZBIT3 | ZBIT2 | ZBIT1 | ZBIT0 |
| Read/Write | R/W |
| After reset | - | - | - | - | - | - | - | - |

Example: Uses Y, Z register as the data pointer to access data in the RAM address 025H of bank0.

```

B0MOV    Y, #00H        ; To set RAM bank 0 for Y register
B0MOV    Z, #25H        ; To set location 25H for Z register
B0MOV    A, @YZ         ; To read a data into ACC
    
```

Example: Uses the Y, Z register as data pointer to clear the RAM data.

```

B0MOV    Y, #0          ; Y = 0, bank 0
B0MOV    Z, #07FH       ; Z = 7FH, the last address of the data memory area
    
```

CLR_YZ_BUF:

```

CLR      @YZ            ; Clear @YZ to be zero

DECMS   Z               ; Z - 1, if Z= 0, finish the routine
JMP     CLR_YZ_BUF     ; Not zero
    
```

```

CLR      @YZ            ; End of clear general purpose data memory area of bank 0
END_CLR:
...
    
```

2.1.15 R REGISTERS

R register is an 8-bit buffer. There are two major functions of the register.

- I Can be used as working register
- I For store high-byte data of look-up table
(MOVC instruction executed, the high-byte data of specified ROM address will be stored in R register and the low-byte data will be stored in ACC).

| 082H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| R | RBIT7 | RBIT6 | RBIT5 | RBIT4 | RBIT3 | RBIT2 | RBIT1 | RBIT0 |
| Read/Write | R/W |
| After reset | - | - | - | - | - | - | - | - |

- **Note: Please refer to the “LOOK-UP TABLE DESCRIPTION” about R register look-up table application.**

2.2 ADDRESSING MODE

2.2.1 IMMEDIATE ADDRESSING MODE

The immediate addressing mode uses an immediate data to set up the location in ACC or specific RAM.

Ø **Example: Move the immediate data 12H to ACC.**

```
MOV      A, #12H      ; To set an immediate data 12H into ACC.
```

Ø **Example: Move the immediate data 12H to R register.**

```
B0MOV   R, #12H      ; To set an immediate data 12H into R register.
```

- **Note: In immediate addressing mode application, the specific RAM must be 0x80~0x87 working register.**

2.2.2 DIRECTLY ADDRESSING MODE

The directly addressing mode moves the content of RAM location in or out of ACC.

Ø **Example: Move 0x12 RAM location data into ACC.**

```
B0MOV   A, 12H      ; To get a content of RAM location 0x12 of bank 0 and save in ACC.
```

Ø **Example: Move ACC data into 0x12 RAM location.**

```
B0MOV   12H, A      ; To get a content of ACC and save in RAM location 12H of bank 0.
```

2.2.3 INDIRECTLY ADDRESSING MODE

The indirectly addressing mode is to access the memory by the data pointer registers (H/L, Y/Z).

Example: Indirectly addressing mode with @HL register

```
B0MOV   H, #0      ; To clear H register to access RAM bank 0.
B0MOV   L, #12H     ; To set an immediate data 12H into L register.
B0MOV   A, @HL      ; Use data pointer @HL reads a data from RAM location
                    ; 012H into ACC.
```

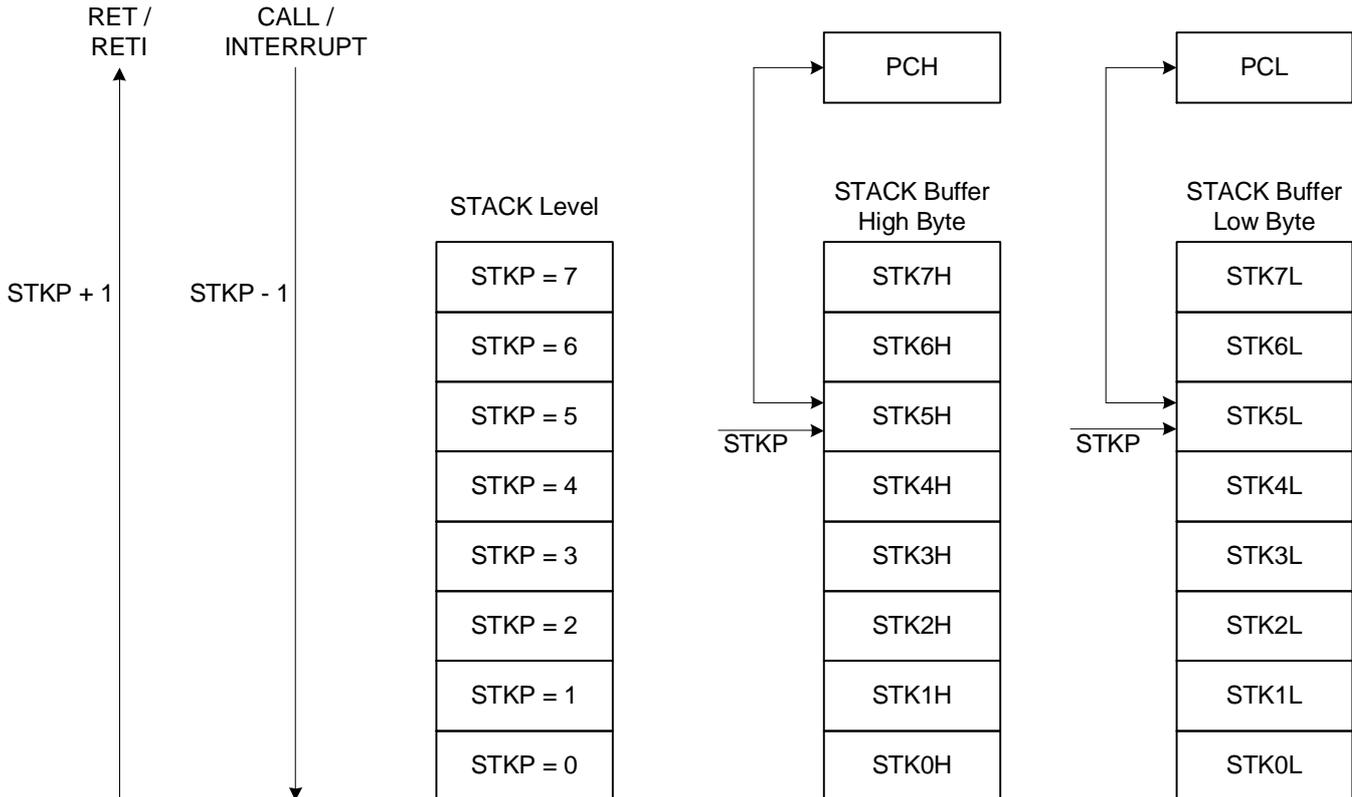
Example: Indirectly addressing mode with @YZ register

```
B0MOV   Y, #0      ; To clear Y register to access RAM bank 0.
B0MOV   Z, #12H     ; To set an immediate data 12H into Z register.
B0MOV   A, @YZ      ; Use data pointer @YZ reads a data from RAM location
                    ; 012H into ACC.
```

2.3 STACK OPERATION

2.3.1 OVERVIEW

The stack buffer has 8-level. These buffers are designed to push and pop up program counter's (PC) data when interrupt service routine and "CALL" instruction are executed. The STKP register is a pointer designed to point active level in order to push or pop up data from stack buffer. The STKnH and STKnL are the stack buffers to store program counter (PC) data.



2.3.2 STACK REGISTERS

The stack pointer (STKP) is a 3-bit register to store the address used to access the stack buffer, 13-bit data memory (STK_nH and STK_nL) set aside for temporary storage of stack addresses.

The two stack operations are writing to the top of the stack (push) and reading from the top of stack (pop). Push operation decrements the STKP and the pop operation increments each time. That makes the STKP always point to the top address of stack buffer and write the last program counter value (PC) into the stack buffer.

The program counter (PC) value is stored in the stack buffer before a CALL instruction executed or during interrupt service routine. Stack operation is a LIFO type (Last in and first out). The stack pointer (STKP) and stack buffer (STK_nH and STK_nL) are located in the system register area bank 0.

| 0DFH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|--------|--------|--------|
| STKP | GIE | - | - | - | - | STKPB2 | STKPB1 | STKPB0 |
| Read/Write | R/W | - | - | - | - | R/W | R/W | R/W |
| After reset | 0 | - | - | - | - | 1 | 1 | 1 |

Bit[2:0] **STKPB_n**: Stack pointer (n = 0 ~ 2)

Bit 7 **GIE**: Global interrupt control bit.
0 = Disable.
1 = Enable. Please refer to the interrupt chapter.

Ø **Example: Stack pointer (STKP) reset, we strongly recommended to clear the stack pointers in the beginning of the program.**

```
MOV     A, #00000111B
B0MOV  STKP, A
```

| 0F0H~0FFH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------|-------|-------|-------|--------|--------|--------|-------|-------|
| STK_nH | - | - | - | SnPC12 | SnPC11 | SnPC10 | SnPC9 | SnPC8 |
| Read/Write | - | - | - | R/W | R/W | R/W | R/W | R/W |
| After reset | - | - | - | 0 | 0 | 0 | 0 | 0 |

| 0F0H~0FFH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| STK_nL | SnPC7 | SnPC6 | SnPC5 | SnPC4 | SnPC3 | SnPC2 | SnPC1 | SnPC0 |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

STK_n = STK_nH , STK_nL (n = 7 ~ 0)

2.3.3 STACK OPERATION EXAMPLE

The two kinds of Stack-Save operations refer to the stack pointer (STKP) and write the content of program counter (PC) to the stack buffer are CALL instruction and interrupt service. Under each condition, the STKP decreases and points to the next available stack location. The stack buffer stores the program counter about the op-code address. The Stack-Save operation is as the following table.

| Stack Level | STKP Register | | | Stack Buffer | | Description |
|-------------|---------------|--------|--------|--------------|----------|-------------------|
| | STKPB2 | STKPB1 | STKPB0 | High Byte | Low Byte | |
| 0 | 1 | 1 | 1 | Free | Free | - |
| 1 | 1 | 1 | 0 | STK0H | STK0L | - |
| 2 | 1 | 0 | 1 | STK1H | STK1L | - |
| 3 | 1 | 0 | 0 | STK2H | STK2L | - |
| 4 | 0 | 1 | 1 | STK3H | STK3L | - |
| 5 | 0 | 1 | 0 | STK4H | STK4L | - |
| 6 | 0 | 0 | 1 | STK5H | STK5L | - |
| 7 | 0 | 0 | 0 | STK6H | STK6L | - |
| 8 | 1 | 1 | 1 | STK7H | STK7L | - |
| > 8 | 1 | 1 | 0 | - | - | Stack Over, error |

There are Stack-Restore operations correspond to each push operation to restore the program counter (PC). The RETI instruction uses for interrupt service routine. The RET instruction is for CALL instruction. When a pop operation occurs, the STKP is incremented and points to the next free stack location. The stack buffer restores the last program counter (PC) to the program counter registers. The Stack-Restore operation is as the following table.

| Stack Level | STKP Register | | | Stack Buffer | | Description |
|-------------|---------------|--------|--------|--------------|----------|-------------|
| | STKPB2 | STKPB1 | STKPB0 | High Byte | Low Byte | |
| 8 | 1 | 1 | 1 | STK7H | STK7L | - |
| 7 | 0 | 0 | 0 | STK6H | STK6L | - |
| 6 | 0 | 0 | 1 | STK5H | STK5L | - |
| 5 | 0 | 1 | 0 | STK4H | STK4L | - |
| 4 | 0 | 1 | 1 | STK3H | STK3L | - |
| 3 | 1 | 0 | 0 | STK2H | STK2L | - |
| 2 | 1 | 0 | 1 | STK1H | STK1L | - |
| 1 | 1 | 1 | 0 | STK0H | STK0L | - |
| 0 | 1 | 1 | 1 | Free | Free | - |

3

RESET

3.1 OVERVIEW

The system would be reset in three conditions as following.

- I Power on reset
- I Watchdog reset
- I Brown out reset
- I External reset (only supports external reset pin enable situation)

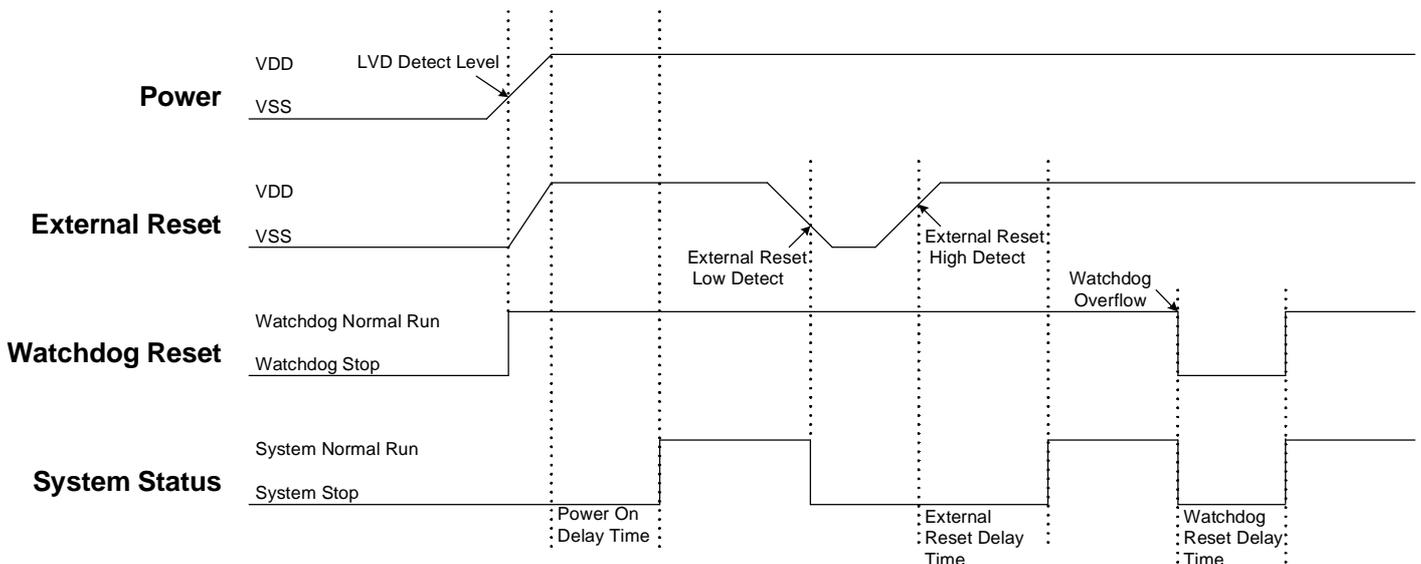
When any reset condition occurs, all system registers keep initial status, program stops and program counter is cleared. After reset status released, the system boots up and program starts to execute from ORG 0. The NT0, NPD flags indicate system reset status. The system can depend on NT0, NPD status and go to different paths by program.

| | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 086H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| PFLAG | NT0 | NPD | - | - | - | C | DC | Z |
| Read/Write | R/W | R/W | - | - | - | R/W | R/W | R/W |
| After reset | - | - | - | - | - | 0 | 0 | 0 |

Bit [7:6] **NT0, NPD**: Reset status flag.

| NT0 | NPD | Condition | Description |
|-----|-----|-------------------------------|--|
| 0 | 0 | Watchdog reset | Watchdog timer overflow. |
| 0 | 1 | Reserved | - |
| 1 | 0 | Power on reset and LVD reset. | Power voltage is lower than LVD detecting level. |
| 1 | 1 | External reset | External reset pin detect low level status. |

Finishing any reset sequence needs some time. The system provides complete procedures to make the power on reset successful. For different oscillator types, the reset time is different. That causes the VDD rise rate and start-up time of different oscillator is not fixed. RC type oscillator's start-up time is very short, but the crystal type is longer. Under client terminal application, users have to take care the power on reset time for the master terminal requirement. The reset timing diagram is as following.



3.2 POWER ON RESET

The power on reset depend no LVD operation for most power-up situations. The power supplying to system is a rising curve and needs some time to achieve the normal voltage. Power on reset sequence is as following.

- I **Power-up:** System detects the power voltage up and waits for power stable.
- I **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- I **System initialization:** All system registers is set as initial conditions and system is ready.
- I **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- I **Program executing:** Power on sequence is finished and program executes from ORG 0.

3.3 WATCHDOG RESET

Watchdog reset is a system protection. In normal condition, system works well and clears watchdog timer by program. Under error condition, system is in unknown situation and watchdog can't be clear by program before watchdog timer overflow. Watchdog timer overflow occurs and the system is reset. After watchdog reset, the system restarts and returns normal mode. Watchdog reset sequence is as following.

- I **Watchdog timer status:** System checks watchdog timer overflow status. If watchdog timer overflow occurs, the system is reset.
- I **System initialization:** All system registers is set as initial conditions and system is ready.
- I **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- I **Program executing:** Power on sequence is finished and program executes from ORG 0.

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- I **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- I **Program executing:** Power on sequence is finished and program executes from ORG 0.

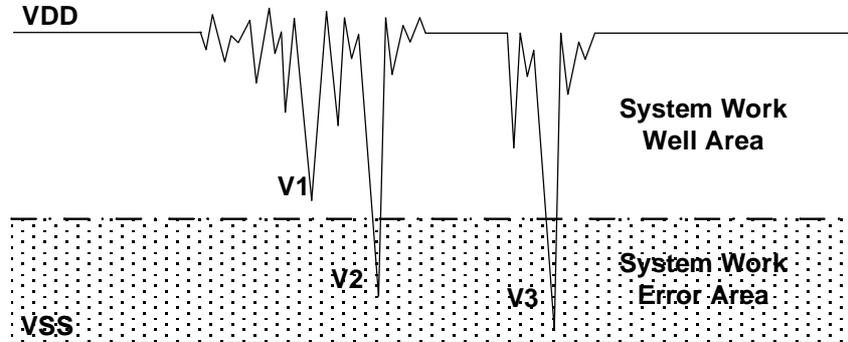
Watchdog timer application note is as following.

- I Before clearing watchdog timer, check I/O status and check RAM contents can improve system error.
- I Don't clear watchdog timer in interrupt vector and interrupt service routine. That can improve main routine fail.
- I Clearing watchdog timer program is only at one part of the program. This way is the best structure to enhance the watchdog timer function.

Note: Please refer to the "WATCHDOG TIMER" about watchdog timer detail information.

3.4 BROWN OUT RESET

The brown out reset is a power dropping condition. The power drops from normal voltage to low voltage by external factors (e.g. EFT interference or external loading changed). The brown out reset would make the system not work well or executing program error.



Brown Out Reset Diagram

The power dropping might through the voltage range that's the system dead-band. The dead-band means the power range can't offer the system minimum operation power requirement. The above diagram is a typical brown out reset diagram. There is a serious noise under the VDD, and VDD voltage drops very deep. There is a dotted line to separate the system working area. The above area is the system work well area. The below area is the system work error area called dead-band. V1 doesn't touch the below area and not effect the system operation. But the V2 and V3 is under the below area and may induce the system error occurrence. Let system under dead-band includes some conditions.

DC application:

The power source of DC application is usually using battery. When low battery condition and MCU drive any loading, the power drops and keeps in dead-band. Under the situation, the power won't drop deeper and not touch the system reset voltage. That makes the system under dead-band.

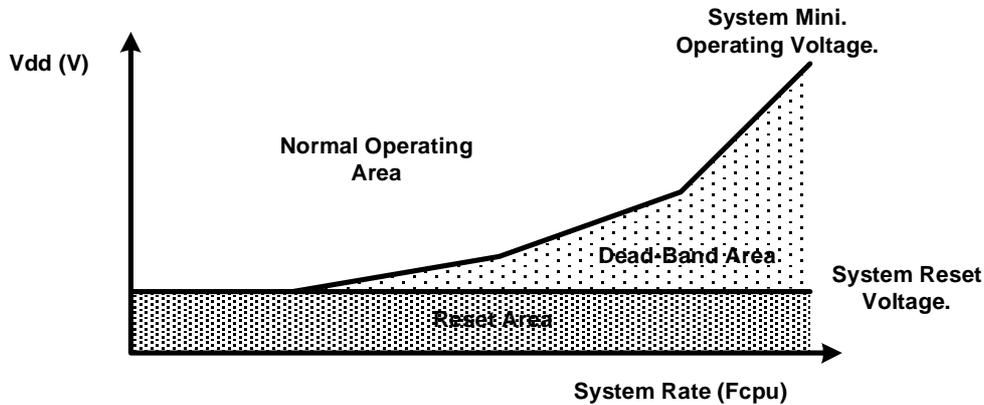
AC application:

In AC power application, the DC power is regulated from AC power source. This kind of power usually couples with AC noise that makes the DC power dirty. Or the external loading is very heavy, e.g. driving motor. The loading operating induces noise and overlaps with the DC power. VDD drops by the noise, and the system works under unstable power situation.

The power on duration and power down duration are longer in AC application. The system power on sequence protects the power on successful, but the power down situation is like DC low battery condition. When turn off the AC power, the VDD drops slowly and through the dead-band for a while.

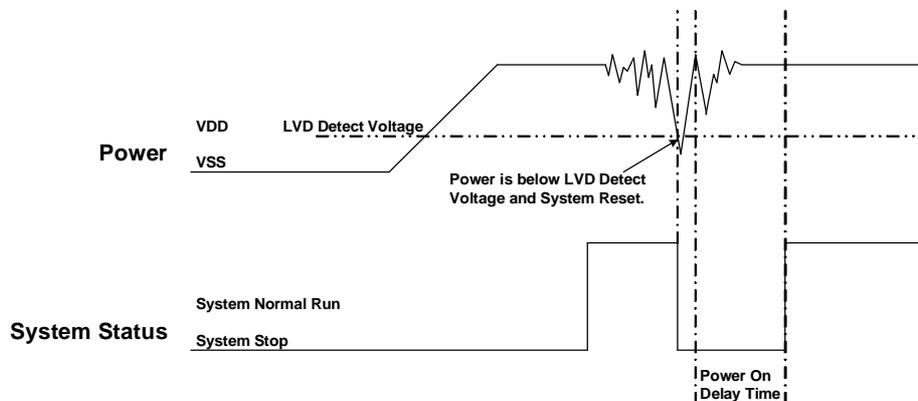
3.5 THE SYSTEM OPERATING VOLTAGE

To improve the brown out reset needs to know the system minimum operating voltage which is depend on the system executing rate and power level. Different system executing rates have different system minimum operating voltage. The electrical characteristic section shows the system voltage to executing rate relationship.



Normally the system operation voltage area is higher than the system reset voltage to VDD, and the reset voltage is decided by LVD detect level. The system minimum operating voltage rises when the system executing rate upper even higher than system reset voltage. The dead-band definition is the system minimum operating voltage above the system reset voltage.

3.6 LOW VOLTAGE DETECTOR (LVD)



The LVD (low voltage detector) is built-in Sonix 8-bit MCU to be brown out reset protection. When the VDD drops and is below LVD detect voltage, the LVD would be triggered, and the system is reset. The LVD detect level is different by each MCU. The LVD voltage level is a point of voltage and not easy to cover all dead-band range. Using LVD to improve brown out reset is depend on application requirement and environment. If the power variation is very deep, violent and trigger the LVD, the LVD can be the protection. If the power variation can touch the LVD detect level and make system work error, the LVD can't be the protection and need to other reset methods. More detail LVD information is in the electrical characteristic section.

3.7 BROWN OUT RESET IMPROVEMENT

How to improve the brown reset condition? There are some methods to improve brown out reset as following.

- I LVD reset
- I Watchdog reset
- I Reduce the system executing rate
- I External reset circuit. (Zener diode reset circuit, Voltage bias reset circuit, External reset IC)

- **Note:**

1. The “ Zener diode reset circuit”, “Voltage bias reset circuit” and “External reset IC” can completely improve the brown out reset, DC low battery and AC slow power down conditions.
2. For AC power application and enhance EFT performance, the system clock is 4MHz/4 (1 mips) and use external reset (“ Zener diode reset circuit”, “Voltage bias reset circuit”, “External reset IC”). The structure can improve noise effective and get good EFT characteristic.

Watchdog reset:

The watchdog timer is a protection to make sure the system executes well. Normally the watchdog timer would be clear at one point of program. Don't clear the watchdog timer in several addresses. The system executes normally and the watchdog won't reset system. When the system is under dead-band and the execution error, the watchdog timer can't be clear by program. The watchdog is continuously counting until overflow occurrence. The overflow signal of watchdog timer triggers the system to reset, and the system return to normal mode after reset sequence. This method also can improve brown out reset condition and make sure the system to return normal mode.

If the system reset by watchdog and the power is still in dead-band, the system reset sequence won't be successful and the system stays in reset status until the power return to normal range.

Reduce the system executing rate:

If the system rate is fast and the dead-band exists, to reduce the system executing rate can improve the dead-band. The lower system rate is with lower minimum operating voltage. Select the power voltage that's no dead-band issue and find out the mapping system rate. Adjust the system rate to the value and the system exits the dead-band issue. This way needs to modify whole program timing to fit the application requirement.

External reset circuit:

The external reset methods also can improve brown out reset and is the complete solution. There are three external reset circuits to improve brown out reset including “Zener diode reset circuit”, “Voltage bias reset circuit” and “External reset IC”. These three reset structures use external reset signal and control to make sure the MCU be reset under power dropping and under dead-band. The external reset information is described in the next section.

3.8 EXTERNAL RESET

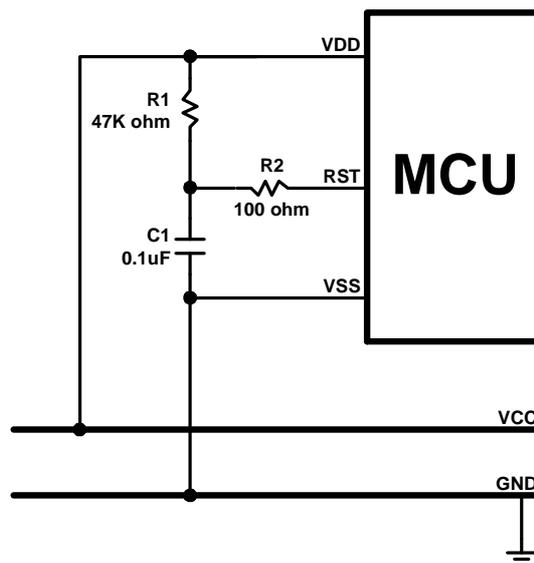
External reset function is controlled by “Reset_Pin” code option. Set the code option as “Reset” option to enable external reset function. External reset pin is Schmitt Trigger structure and low level active. The system is running when reset pin is high level voltage input. The reset pin receives the low voltage and the system is reset. The external reset operation activates in power on and normal running mode. During system power-up, the external reset pin must be high level input, or the system keeps in reset status. External reset sequence is as following.

- I **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- I **System initialization:** All system registers is set as initial conditions and system is ready.
- I **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- I **Program executing:** Power on sequence is finished and program executes from ORG 0.

The external reset can reset the system during power on duration, and good external reset circuit can protect the system to avoid working at unusual power condition, e.g. brown out reset in AC power application...

3.9 EXTERNAL RESET CIRCUIT

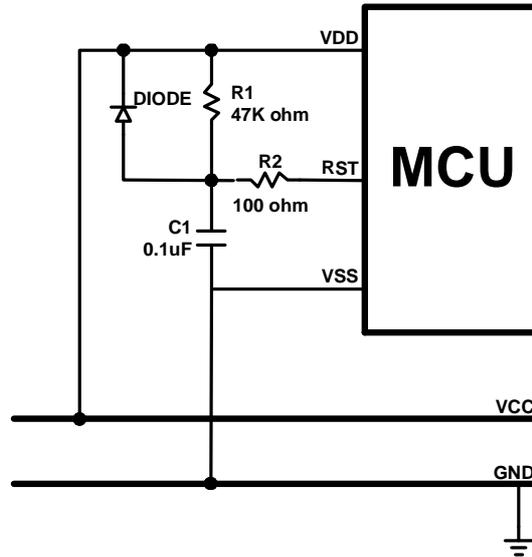
3.9.1 Simply RC Reset Circuit



This is the basic reset circuit, and only includes R1 and C1. The RC circuit operation makes a slow rising signal into reset pin as power up. The reset signal is slower than VDD power up timing, and system occurs a power on signal from the timing difference.

- **Note:** The reset circuit is no any protection against unusual power or brown out reset.

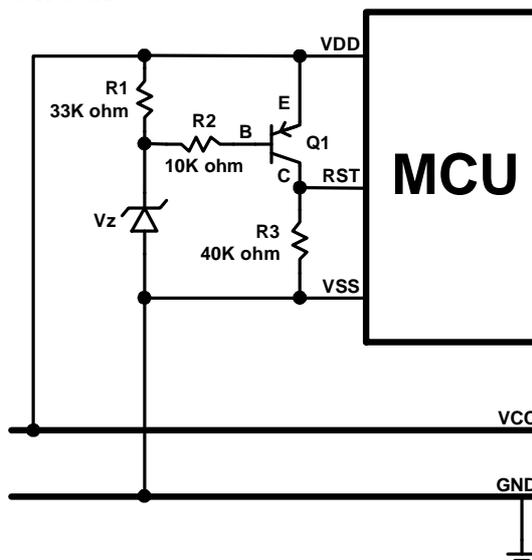
3.9.2 Diode & RC Reset Circuit



This is the better reset circuit. The R1 and C1 circuit operation is like the simply reset circuit to make a power on signal. The reset circuit has a simply protection against unusual power. The diode offers a power positive path to conduct higher power to VDD. It is can make reset pin voltage level to synchronize with VDD voltage. The structure can improve slight brown out reset condition.

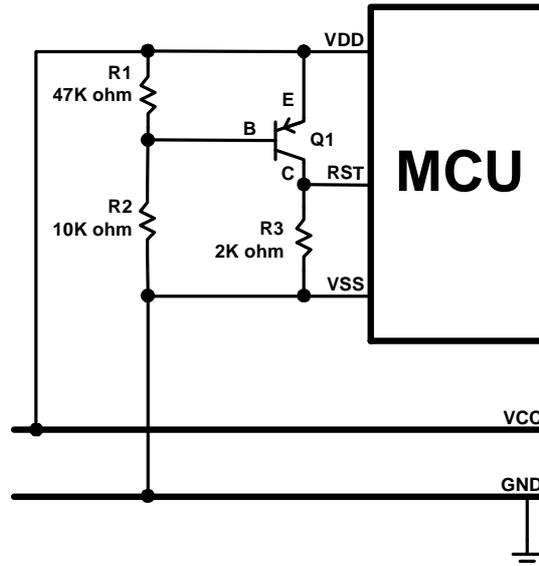
- **Note:** The R2 100 ohm resistor of “Simply reset circuit” and “Diode & RC reset circuit” is necessary to limit any current flowing into reset pin from external capacitor C in the event of reset pin breakdown due to Electrostatic Discharge (ESD) or Electrical Over-stress (EOS).

3.9.3 Zener Diode Reset Circuit



The zener diode reset circuit is a simple low voltage detector and can **improve brown out reset condition completely**. Use zener voltage to be the active level. When VDD voltage level is above “ $V_z + 0.7V$ ”, the C terminal of the PNP transistor outputs high voltage and MCU operates normally. When VDD is below “ $V_z + 0.7V$ ”, the C terminal of the PNP transistor outputs low voltage and MCU is in reset mode. Decide the reset detect voltage by zener specification. Select the right zener voltage to conform the application.

3.9.4 Voltage Bias Reset Circuit

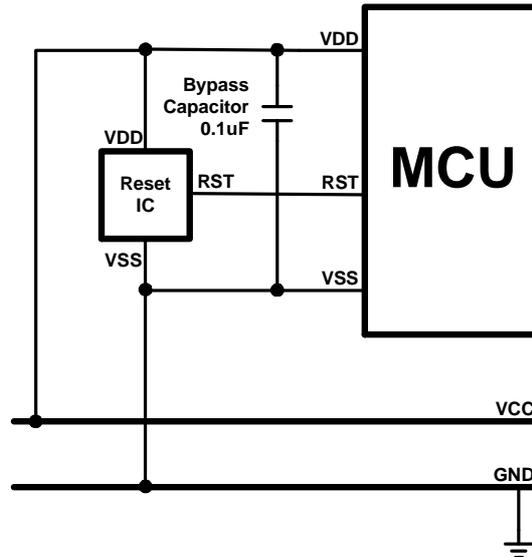


The voltage bias reset circuit is a low cost voltage detector and can **improve brown out reset condition completely**. The operating voltage is not accurate as zener diode reset circuit. Use R1, R2 bias voltage to be the active level. When VDD voltage level is above or equal to $0.7V \times (R1 + R2) / R1$, the C terminal of the PNP transistor outputs high voltage and MCU operates normally. When VDD is below $0.7V \times (R1 + R2) / R1$, the C terminal of the PNP transistor outputs low voltage and MCU is in reset mode.

Decide the reset detect voltage by R1, R2 resistances. Select the right R1, R2 value to conform the application. In the circuit diagram condition, the MCU's reset pin level varies with VDD voltage variation, and the differential voltage is 0.7V. If the VDD drops and the voltage lower than reset pin detect level, the system would be reset. If want to make the reset active earlier, set the $R2 > R1$ and the cap between VDD and C terminal voltage is larger than 0.7V. The external reset circuit is with a stable current through R1 and R2. For power consumption issue application, e.g. DC power system, the current must be considered to whole system power consumption.

- **Note:** Under unstable power condition as brown out reset, "Zener diode rest circuit" and "Voltage bias reset circuit" can protects system no any error occurrence as power dropping. When power drops below the reset detect voltage, the system reset would be triggered, and then system executes reset sequence. That makes sure the system work well under unstable power situation.

3.9.5 External Reset IC



The external reset circuit also use external reset IC to enhance MCU reset performance. This is a high cost and good effect solution. By different application and system requirement to select suitable reset IC. The reset circuit can improve all power variation.

4 SYSTEM CLOCK

4.1 OVERVIEW

The micro-controller is a dual clock system. There are high-speed clock and low-speed clock. The high-speed clock is generated from the external oscillator circuit. The low-speed clock is generated from on-chip low-speed RC oscillator circuit (ILRC 16KHz @3V, 32KHz @5V).

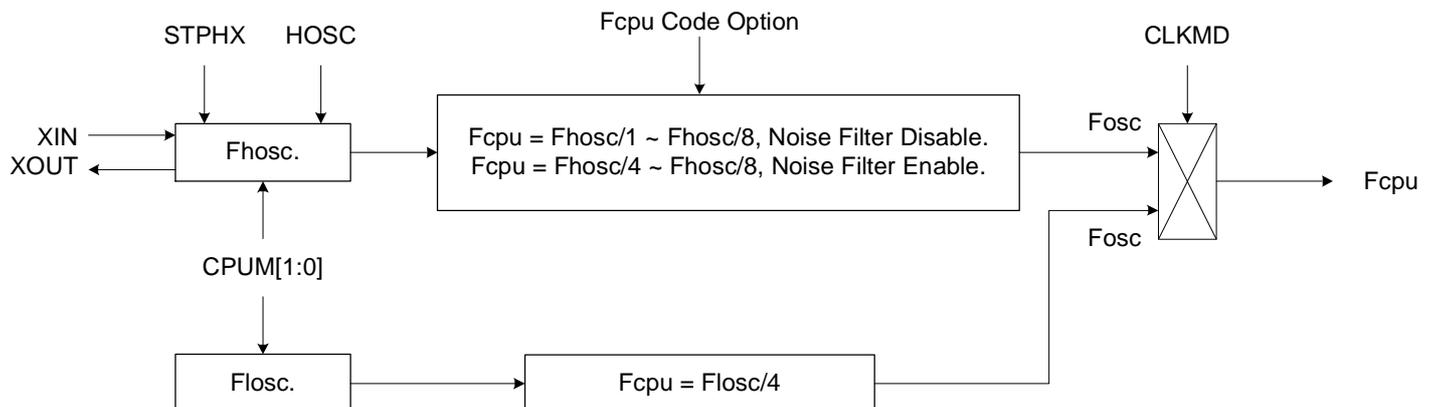
Both the high-speed clock and the low-speed clock can be system clock (Fosc). The system clock in slow mode is divided by 4 to be the instruction cycle (Fcpu).

F Normal Mode (High Clock): $F_{cpu} = F_{osc} / N$, $N = 1 \sim 8$, Select N by Fcpu code option.

F Slow Mode (Low Clock): $F_{cpu} = F_{osc}/4$.

SONiX provides a “Noise Filter” controlled by code option. In high noisy situation, the noise filter can isolate noise outside and protect system works well. The minimum Fcpu of high clock is limited at **Fosc/4** when noise filter enable.

4.2 CLOCK BLOCK DIAGRAM



- I HOSC: High_Clk code option.
- I Fosc: External high-speed clock.
- I Fosc: Internal low-speed RC clock (about 16KHz@3V, 32KHz@5V).
- I Fosc: System clock source.
- I Fcpu: Instruction cycle.

4.3 OSCM REGISTER

The OSCM register is an oscillator control register. It controls oscillator status, system mode.

| OCAH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| OSCM | 0 | 0 | 0 | CPUM1 | CPUM0 | CLKMD | STPHX | 0 |
| Read/Write | - | - | - | R/W | R/W | R/W | R/W | - |
| After reset | - | - | - | 0 | 0 | 0 | 0 | - |

- Bit 1 **STPHX**: External high-speed oscillator control bit.
 0 = External high-speed oscillator free run.
 1 = External high-speed oscillator free run stop. Internal low-speed RC oscillator is still running.
- Bit 2 **CLKMD**: System high/Low clock mode control bit.
 0 = Normal (dual) mode. System clock is high clock.
 1 = Slow mode. System clock is internal low clock.
- Bit[4:3] **CPUM[1:0]**: CPU operating mode control bits.
 00 = normal.
 01 = sleep (power down) mode.
 10 = green mode.
 11 = reserved.

Ø Example: Stop high-speed oscillator

```
B0BSET    FSTPHX            ; To stop external high-speed oscillator only.
```

Ø Example: When entering the power down mode (sleep mode), both high-speed oscillator and internal low-speed oscillator will be stopped.

```
B0BSET    FCPUM0            ; To stop external high-speed oscillator and internal low-speed  

                              ; oscillator called power down mode (sleep mode).
```

4.4 SYSTEM HIGH CLOCK

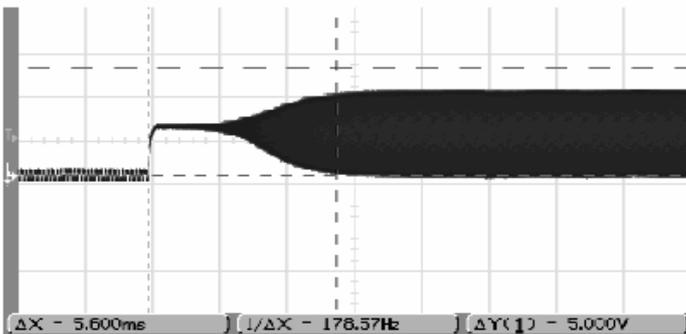
The system high clock is from external oscillator. The high clock type is controlled by “High_Clk” code option.

| High_Clk Code Option | Description |
|----------------------|---|
| RC | The high clock is external RC type oscillator. XOUT pin is general purpose I/O pin. |
| 12M | The high clock is external high speed oscillator. The typical frequency is 12MHz. |
| 4M | The high clock is external oscillator. The typical frequency is 4MHz. |

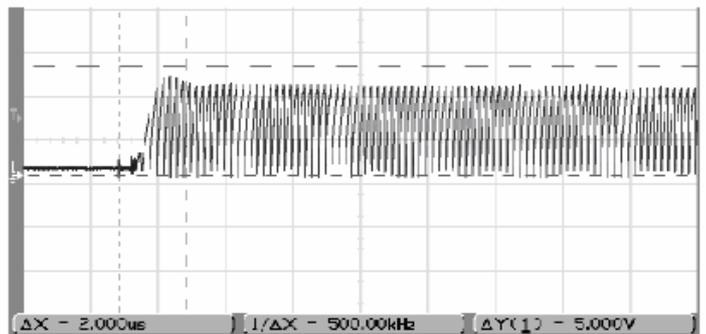
4.4.1 EXTERNAL HIGH CLOCK

External high clock includes three modules (Crystal/Ceramic, RC and external clock signal). The high clock oscillator module is controlled by High_Clk code option. The start up time of crystal/ceramic and RC type oscillator is different. RC type oscillator’s start-up time is very short, but the crystal’s is longer. The oscillator start-up time decides reset time length.

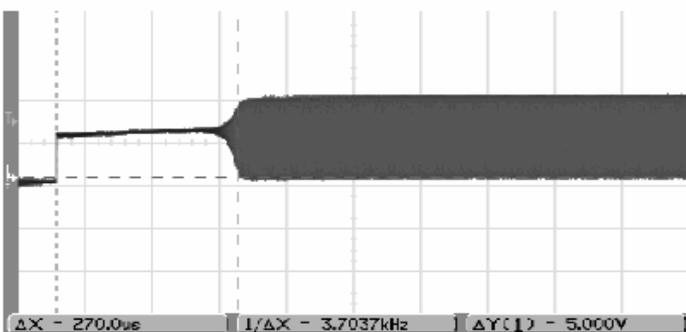
4MHz Crystal



RC

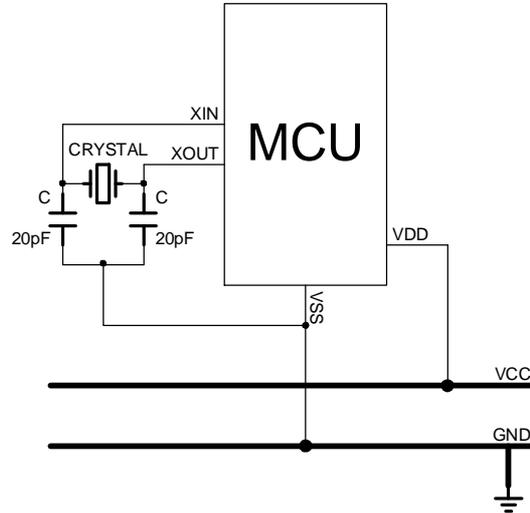


4MHz Ceramic



4.4.1.1 CRYSTAL/CERAMIC

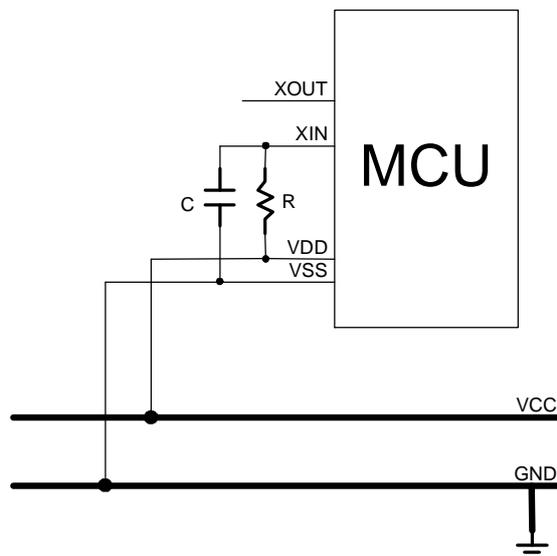
Crystal/Ceramic devices are driven by XIN, XOUT pins. For high/normal/low frequency, the driving currents are different. High_Clk code option supports different frequencies. 12M option is for high speed (ex. 12MHz). 4M option is for normal speed (ex. 4MHz).



- **Note:** Connect the Crystal/Ceramic and C as near as possible to the XIN/XOUT/VSS pins of micro-controller.

4.4.1.2 RC

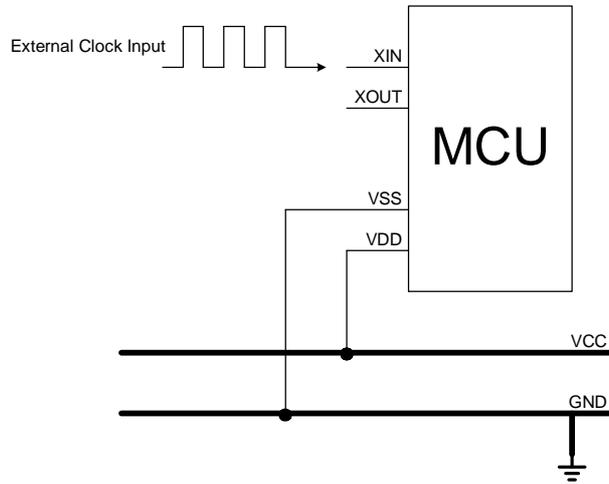
Selecting RC oscillator is by RC option of High_Clk code option. RC type oscillator's frequency is up to 10MHz. Using "R" value is to change frequency. 50P~100P is good value for "C". XOUT pin is general purpose I/O pin.



- **Note:** Connect the R and C as near as possible to the VDD pin of micro-controller.

4.4.1.3 EXTERNAL CLOCK SIGNAL

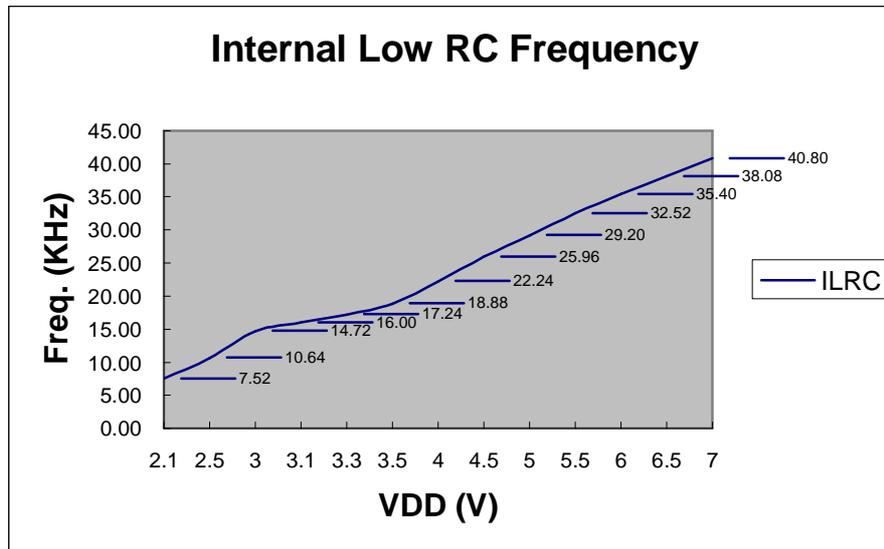
Selecting external clock signal input to be system clock is by RC option of High_Clk code option. The external clock signal is input from XIN pin. XOUT pin is general purpose I/O pin.



- **Note: The GND of external oscillator circuit must be as near as possible to VSS pin of micro-controller.**

4.5 SYSTEM LOW CLOCK

The system low clock source is the internal low-speed oscillator built in the micro-controller. The low-speed oscillator uses RC type oscillator circuit. The frequency is affected by the voltage and temperature of the system. In common condition, the frequency of the RC oscillator is about 16KHz at 3V and 32KHz at 5V. The relation between the RC frequency and voltage is as the following figure.



The internal low RC supports watchdog clock source and system slow mode controlled by CLKMD.

F $F_{osc} = \text{Internal low RC oscillator (about 16KHz @3V, 32KHz @5V)}$.

F $\text{Slow mode } F_{cpu} = F_{osc} / 4$

There are two conditions to stop internal low RC. One is power down mode, and the other is green mode of 32K mode and watchdog disable. If system is in 32K mode and watchdog disable, only 32K oscillator activates and system is under low power consumption.

Ø **Example: Stop internal low-speed oscillator by power down mode.**

```
B0BSET   FCPUM0           ; To stop external high-speed oscillator and internal low-speed
                                ; oscillator called power down mode (sleep mode).
```

- **Note: The internal low-speed clock can't be turned off individually. It is controlled by CPUM0, CPUM1 (32K, watchdog disable) bits of OSCM register.**

4.5.1 SYSTEM CLOCK MEASUREMENT

Under design period, the users can measure system clock speed by software instruction cycle (Fcpu). This way is useful in RC mode.

Ø **Example: Fcpu instruction cycle of external oscillator.**

```
B0BSET    P0M.0           ; Set P0.0 to be output mode for outputting Fcpu toggle signal.
```

@ @:

```
B0BSET    P0.0           ; Output Fcpu toggle signal in low-speed clock mode.
B0BCLR    P0.0           ; Measure the Fcpu frequency by oscilloscope.
JMP       @B
```

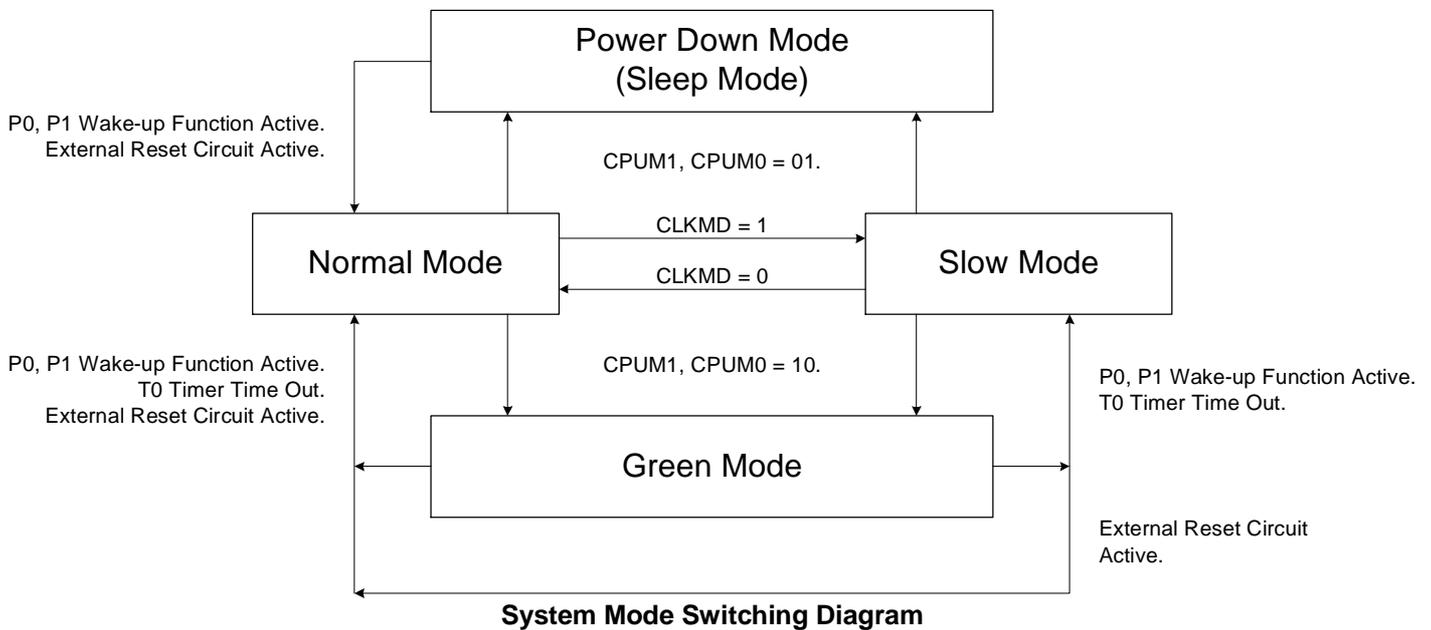
- **Note: Do not measure the RC frequency directly from XIN; the probe impedance will affect the RC frequency.**

5 SYSTEM OPERATION MODE

5.1 OVERVIEW

The chip is featured with low power consumption by switching around four different modes as following.

- I Normal mode (High-speed mode)
- I Slow mode (Low-speed mode)
- I Power-down mode (Sleep mode)
- I Green mode



Operating mode description

| MODE | NORMAL | SLOW | GREEN | POWER DOWN (SLEEP) | REMARK |
|--------------------|--------------------------|--------------------------|--------------------------|--------------------------|----------------------------------|
| EHOSC | Running | By STPHX | By STPHX | Stop | |
| ILRC | Running | Running | Running | Stop | |
| CPU instruction | Executing | Executing | Stop | Stop | |
| T0 timer | *Active | *Active | *Active | Inactive | * Active if T0ENB=1 |
| TC1 timer | *Active | *Active | *Active | Inactive | * Active if TC1ENB=1 |
| Watchdog timer | By Watch_Dog Code option | Refer to code option description |
| Internal interrupt | All active | All active | T0, TC1 | All inactive | |
| External interrupt | All active | All active | All active | All inactive | |
| Wakeup source | - | - | P0, P1, T0 Reset | P0, P1, Reset | |

EHOSC: External high clock

ILRC: Internal low clock (16K RC oscillator at 3V, 32K at 5V)

5.2 SYSTEM MODE SWITCHING

Ø Example: Switch normal/slow mode to power down (sleep) mode.

```
BOBSET          FCPUM0          ; Set CPUM0 = 1.
```

- **Note: During the sleep, only the wakeup pin and reset can wakeup the system back to the normal mode.**

Ø Example: Switch normal mode to slow mode.

```
BOBSET          FCLKMD          ;To set CLKMD = 1, Change the system into slow mode
BOBSET          FSTPHX          ;To stop external high-speed oscillator for power saving.
```

Ø Example: Switch slow mode to normal mode (The external high-speed oscillator is still running)

```
BOBCLR          FCLKMD          ;To set CLKMD = 0
```

Ø Example: Switch slow mode to normal mode (The external high-speed oscillator stops)

If external high clock stop and program want to switch back normal mode. It is necessary to delay at least 20ms for external clock stable.

```
BOBCLR          FSTPHX          ; Turn on the external high-speed oscillator.
@@:             BOMOV           Z, #54          ; If VDD = 5V, internal RC=32KHz (typical) will delay
                DECMS           Z             ; 0.125ms X 162 = 20.25ms for external clock stable
                JMP             @B
BOBCLR          FCLKMD          ; Change the system back to the normal mode
```

Ø Example: Switch normal/slow mode to green mode.

```
BOBSET          FCPUM1          ; Set CPUM1 = 1.
```

- **Note: If T0 timer wakeup function is disabled in the green mode, only the wakeup pin and reset pin can wakeup the system backs to the previous operation mode.**

Ø Example: Switch normal/slow mode to Green mode and enable T0 wakeup function.

; Set T0 timer wakeup function.

| | | |
|---------------|---------------|---|
| B0BCLR | FT0IEN | ; To disable T0 interrupt service |
| B0BCLR | FT0ENB | ; To disable T0 timer |
| MOV | A,#20H | ; |
| B0MOV | T0M,A | ; To set T0 clock = Fcpu / 64 |
| MOV | A,#74H | ; |
| B0MOV | T0C,A | ; To set T0C initial value = 74H (To set T0 interval = 10 ms) |
| B0BCLR | FT0IEN | ; To disable T0 interrupt service |
| B0BCLR | FT0IRQ | ; To clear T0 interrupt request |
| B0BSET | FT0ENB | ; To enable T0 timer |

; Go into green mode

| | | |
|--------|--------|--------------------|
| B0BCLR | FCPUM0 | ;To set CPUMx = 10 |
| B0BSET | FCPUM1 | |

- **Note: During the green mode with T0 wake-up function, the wakeup pins, reset pin and T0 can wakeup the system back to the last mode. T0 wake-up period is controlled by program and T0ENB must be set.**

5.3 WAKEUP

5.3.1 OVERVIEW

Under power down mode (sleep mode) or green mode, program doesn't execute. The wakeup trigger can wake the system up to normal mode or slow mode. The wakeup trigger sources are external trigger (P0, P1 level change) and internal trigger (T0 timer overflow).

- I Power down mode is waked up to normal mode. The wakeup trigger is only external trigger (P0, P1 level change)
- I Green mode is waked up to last mode (normal mode or slow mode). The wakeup triggers are external trigger (P0, P1 level change) and internal trigger (T0 timer overflow).

5.3.2 WAKEUP TIME

When the system is in power down mode (sleep mode), the high clock oscillator stops. When waked up from power down mode, MCU waits for 2048 external high-speed oscillator clocks as the wakeup time to stable the oscillator circuit. After the wakeup time, the system goes into the normal mode.

- **Note: Wakeup from green mode is no wakeup time because the clock doesn't stop in green mode.**

The value of the wakeup time is as the following.

The Wakeup time = $1/F_{osc} * 2048$ (sec) + high clock start-up time

- **Note: The high clock start-up time is depended on the VDD and oscillator type of high clock.**

Example: In power down mode (sleep mode), the system is waked up. After the wakeup time, the system goes into normal mode. The wakeup time is as the following.

***The wakeup time = $1/F_{osc} * 2048 = 0.512$ ms (Fosc = 4MHz)
The total wakeup time = 0.512 ms + oscillator start-up time***

5.3.3 P1W WAKEUP CONTROL REGISTER

Under power down mode (sleep mode) and green mode, the I/O ports with wakeup function are able to wake the system up to normal mode. The Port 0 and Port 1 have wakeup function. Port 0 wakeup function always enables, but the Port 1 is controlled by the P1W register.

| 0C0H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P1W | P17W | P16W | P15W | P14W | P13W | P12W | P11W | P10W |
| Read/Write | W | W | W | W | W | W | W | W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit[7:0] **P10W~P17W**: Port 1 wakeup function control bits.

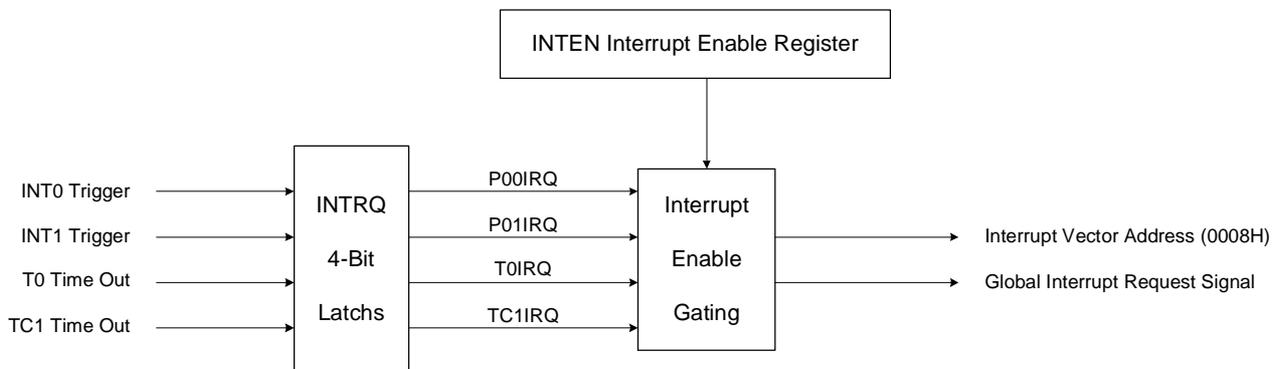
0 = Disable P1n wakeup function.

1 = Enable P1n wakeup function.

6 INTERRUPT

6.1 OVERVIEW

This MCU provides three interrupt sources, including two internal interrupt (T0/TC1) and two external interrupt (INT0, INT1). The external interrupt can wakeup the chip while the system is switched from power down mode to high-speed normal mode. Once interrupt service is executed, the GIE bit in STKP register will clear to “0” for stopping other interrupt request. On the contrast, when interrupt service exits, the GIE bit will set to “1” to accept the next interrupts’ request. All of the interrupt request signals are stored in INTRQ register.



Note: The GIE bit must enable during all interrupt operation.

6.2 INTEN INTERRUPT ENABLE REGISTER

INTEN is the interrupt request control register including one internal interrupts, one external interrupts enable control bits. One of the register to be set "1" is to enable the interrupt request function. Once of the interrupt occur, the stack is incremented and program jump to ORG 8 to execute interrupt service routines. The program exits the interrupt service routine when the returning interrupt service routine instruction (RETI) is executed.

| 0C9H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------|-------|--------|-------|-------|-------|-------|--------|--------|
| INTEN | - | TC1IEN | - | TOIEN | - | - | P01IEN | P00IEN |
| Read/Write | - | R/W | - | R/W | - | - | R/W | R/W |
| After reset | - | 0 | - | 0 | - | - | 0 | 0 |

Bit 0 **P00IEN:** External P0.0 interrupt (INT0) control bit.
0 = Disable INT0 interrupt function.
1 = Enable INT0 interrupt function.

Bit 1 **P01IEN:** External P0.1 interrupt (INT1) control bit.
0 = Disable INT1 interrupt function.
1 = Enable INT1 interrupt function.

Bit 4 **TOIEN:** T0 timer interrupt control bit.
0 = Disable T0 interrupt function.
1 = Enable T0 interrupt function.

Bit 6 **TC1IEN:** TC1 timer interrupt control bit.
0 = Disable TC1 interrupt function.
1 = Enable TC1 interrupt function.

6.3 INTRQ INTERRUPT REQUEST REGISTER

INTRQ is the interrupt request flag register. The register includes all interrupt request indication flags. Each one of the interrupt requests occurs, the bit of the INTRQ register would be set "1". The INTRQ value needs to be clear by programming after detecting the flag. In the interrupt vector of program, users know the any interrupt requests occurring by the register and do the routine corresponding of the interrupt request.

| 0C8H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------|-------|--------|-------|-------|-------|-------|--------|--------|
| INTRQ | - | TC1IRQ | - | T0IRQ | - | - | P01IRQ | P00IRQ |
| Read/Write | - | R/W | - | R/W | - | - | R/W | R/W |
| After reset | - | 0 | - | 0 | - | - | 0 | 0 |

Bit 0 **P00IRQ**: External P0.0 interrupt (INT0) request flag.
0 = None INT0 interrupt request.
1 = INT0 interrupt request.

Bit 1 **P01IRQ**: External P0.1 interrupt (INT1) request flag.
0 = None INT1 interrupt request.
1 = INT1 interrupt request.

Bit 4 **T0IRQ**: T0 timer interrupt request flag.
0 = None T0 interrupt request.
1 = T0 interrupt request.

Bit 6 **TC1IRQ**: TC1 timer interrupt request flag.
0 = None TC1 interrupt request.
1 = TC1 interrupt request.

6.4 GIE GLOBAL INTERRUPT OPERATION

GIE is the global interrupt control bit. All interrupts start work after the GIE = 1 It is necessary for interrupt service request. One of the interrupt requests occurs, and the program counter (PC) points to the interrupt vector (ORG 8) and the stack add 1 level.

| 0DFH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|--------|--------|--------|
| STKP | GIE | - | - | - | - | STKPB2 | STKPB1 | STKPB0 |
| Read/Write | R/W | - | - | - | - | R/W | R/W | R/W |
| After reset | 0 | - | - | - | - | 1 | 1 | 1 |

Bit 7 **GIE**: Global interrupt control bit.
0 = Disable global interrupt.
1 = Enable global interrupt.

Ø **Example: Set global interrupt control bit (GIE).**

BOBSET FGIE ; Enable GIE

- **Note: The GIE bit must enable during all interrupt operation.**

6.5 PUSH, POP ROUTINE

When any interrupt occurs, system will jump to ORG 8 and execute interrupt service routine. It is necessary to save ACC, PFLAG data. The chip includes "PUSH", "POP" for in/out interrupt service routine. The two instructions save and load ACC, PFLAG data into buffers and avoid main routine error after interrupt service routine finishing.

Note: "PUSH", "POP" instructions save and load ACC/PFLAG without (NT0, NPD). PUSH/POP buffer is an unique buffer and only one level.

Example: Store ACC and PAFLG data by PUSH, POP instructions when interrupt service routine executed.

```

                ORG      0
                JMP      START

                ORG      8
                JMP      INT_SERVICE

START:         ORG      10H
                ...

INT_SERVICE:  PUSH          ; Save ACC and PFLAG to buffers.
                ...
                ...
                POP          ; Load ACC and PFLAG from buffers.
                RETI        ; Exit interrupt service vector
                ...
                ENDP

```

6.6 INTO (P0.0) INTERRUPT OPERATION

When the INTO trigger occurs, the P00IRQ will be set to “1” no matter the P00IEN is enable or disable. If the P00IEN = 1 and the trigger event P00IRQ is also set to be “1”. As the result, the system will execute the interrupt vector (ORG 8). If the P00IEN = 0 and the trigger event P00IRQ is still set to be “1”. Moreover, the system won’t execute interrupt vector even when the P00IRQ is set to be “1”. Users need to be cautious with the operation under multi-interrupt situation.

- **Note: The interrupt trigger direction of P0.0 is control by PEDGE register.**

| 0BFH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| PEDGE | - | - | - | P00G1 | P00G0 | - | - | - |
| Read/Write | - | - | - | R/W | R/W | - | - | - |
| After reset | - | - | - | 1 | 0 | - | - | - |

Bit[4:3] **P00G[1:0]**: P0.0 interrupt trigger edge control bits.
 00 = reserved.
 01 = rising edge.
 10 = falling edge.
 11 = rising/falling bi-direction (Level change trigger).

Ø **Example: Setup INTO interrupt request and bi-direction edge trigger.**

```

MOV      A, #18H
BOMOV   PEDGE, A      ; Set INTO interrupt trigger as bi-direction edge.

B0BSET  FP00IEN       ; Enable INTO interrupt service
B0BCLR  FP00IRQ       ; Clear INTO interrupt request flag
B0BSET  FGIE          ; Enable GIE
  
```

Ø **Example: INTO interrupt service routine.**

```

ORG      8             ; Interrupt vector
JMP     INT_SERVICE

INT_SERVICE:
...
; Push routine to save ACC and PFLAG to buffers.

B0BTS1  FP00IRQ       ; Check P00IRQ
JMP     EXIT_INT      ; P00IRQ = 0, exit interrupt vector

B0BCLR  FP00IRQ       ; Reset P00IRQ
...
; INTO interrupt service routine
...

EXIT_INT:
...
; Pop routine to load ACC and PFLAG from buffers.

RETI
; Exit interrupt vector
  
```

6.7 INT1 (P0.1) INTERRUPT OPERATION

When the INT1 trigger occurs, the P01IRQ will be set to “1” no matter the P01IEN is enable or disable. If the P01IEN = 1 and the trigger event P01IRQ is also set to be “1”. As the result, the system will execute the interrupt vector (ORG 8). If the P01IEN = 0 and the trigger event P01IRQ is still set to be “1”. Moreover, the system won't execute interrupt vector even when the P01IRQ is set to be “1”. Users need to be cautious with the operation under multi-interrupt situation.

- **Note: The interrupt trigger direction of P0.1 is falling edge.**

Example: INT1 interrupt request setup.

```

B0BSET      FP01IEN      ; Enable INT1 interrupt service
B0BCLR      FP01IRQ      ; Clear INT1 interrupt request flag
B0BSET      FGIE         ; Enable GIE

```

Example: INT1 interrupt service routine.

```

ORG          8           ; Interrupt vector
INT_SERVICE:
  JMP        INT_SERVICE

  ...                   ; Push routine to save ACC and PFLAG to buffers.

  B0BTS1     FP01IRQ      ; Check P01IRQ
  JMP        EXIT_INT     ; P01IRQ = 0, exit interrupt vector

  B0BCLR     FP01IRQ      ; Reset P01IRQ
  ...                   ; INT1 interrupt service routine
  ...

EXIT_INT:
  ...                   ; Pop routine to load ACC and PFLAG from buffers.

  RETI        ; Exit interrupt vector

```

6.8 T0 INTERRUPT OPERATION

When the T0C counter occurs overflow, the T0IRQ will be set to "1" however the T0IEN is enable or disable. If the T0IEN = 1, the trigger event will make the T0IRQ to be "1" and the system enter interrupt vector. If the T0IEN = 0, the trigger event will make the T0IRQ to be "1" but the system will not enter interrupt vector. Users need to care for the operation under multi-interrupt situation.

Ø Example: T0 interrupt request setup.

```

B0BCLR    FT0IEN    ; Disable T0 interrupt service
B0BCLR    FT0ENB    ; Disable T0 timer
MOV       A, #20H   ;
B0MOV     T0M, A    ; Set T0 clock = Fcpu / 64
MOV       A, #74H   ; Set T0C initial value = 74H
B0MOV     T0C, A    ; Set T0 interval = 10 ms

B0BSET    FT0IEN    ; Enable T0 interrupt service
B0BCLR    FT0IRQ    ; Clear T0 interrupt request flag
B0BSET    FT0ENB    ; Enable T0 timer

B0BSET    FGIE      ; Enable GIE

```

Example: T0 interrupt service routine.

```

ORG       8          ; Interrupt vector
JMP      INT_SERVICE
INT_SERVICE:
...
; Push routine to save ACC and PFLAG to buffers.

B0BTS1   FT0IRQ    ; Check T0IRQ
JMP     EXIT_INT  ; T0IRQ = 0, exit interrupt vector

B0BCLR   FT0IRQ    ; Reset T0IRQ
MOV     A, #74H    ; Reset T0C.
B0MOV    T0C, A    ; T0 interrupt service routine
...
EXIT_INT:
...
; Pop routine to load ACC and PFLAG from buffers.

RETI     ; Exit interrupt vector

```

6.9 TC1 INTERRUPT OPERATION

When the TC1C counter overflows, the TC1IRQ will be set to "1" no matter the TC1IEN is enable or disable. If the TC1IEN and the trigger event TC1IRQ is set to be "1". As the result, the system will execute the interrupt vector. If the TC1IEN = 0, the trigger event TC1IRQ is still set to be "1". Moreover, the system won't execute interrupt vector even when the TC1IEN is set to be "1". Users need to be cautious with the operation under multi-interrupt situation.

Example: TC1 interrupt request setup.

```

B0BCLR    FTC1IEN    ; Disable TC1 interrupt service
B0BCLR    FTC1ENB    ; Disable TC1 timer
MOV       A, #20H    ;
B0MOV     TC1M, A    ; Set TC1 clock = Fcpu / 64
MOV       A, #74H    ; Set TC1C initial value = 74H
B0MOV     TC1C, A    ; Set TC1 interval = 10 ms

B0BSET    FTC1IEN    ; Enable TC1 interrupt service
B0BCLR    FTC1IRQ    ; Clear TC1 interrupt request flag
B0BSET    FTC1ENB    ; Enable TC1 timer

B0BSET    FGIE       ; Enable GIE

```

Example: TC1 interrupt service routine.

```

ORG       8          ; Interrupt vector
JMP      INT_SERVICE

INT_SERVICE:

...          ; Push routine to save ACC and PFLAG to buffers.

B0BTS1    FTC1IRQ    ; Check TC1IRQ
JMP      EXIT_INT   ; TC1IRQ = 0, exit interrupt vector

B0BCLR    FTC1IRQ    ; Reset TC1IRQ
MOV       A, #74H    ;
B0MOV     TC1C, A    ; Reset TC1C.
...          ; TC1 interrupt service routine
...

EXIT_INT:

...          ; Pop routine to load ACC and PFLAG from buffers.

RETI      ; Exit interrupt vector

```

6.10 MULTI-INTERRUPT OPERATION

Under certain condition, the software designer uses more than one interrupt requests. Processing multi-interrupt request requires setting the priority of the interrupt requests. The IRQ flags of interrupts are controlled by the interrupt event. Nevertheless, the IRQ flag "1" doesn't mean the system will execute the interrupt vector. In addition, which means the IRQ flags can be set "1" by the events without enable the interrupt. Once the event occurs, the IRQ will be logic "1". The IRQ and its trigger event relationship is as the below table.

| <i>Interrupt Name</i> | <i>Trigger Event Description</i> |
|-----------------------|-----------------------------------|
| P00IRQ | P0.0 trigger controlled by PEDGE. |
| P01IRQ | P0.1 falling edge trigger. |
| T0IRQ | T0C overflow. |
| TC1IRQ | TC1C overflow. |

For multi-interrupt conditions, two things need to be taking care of. One is to set the priority for these interrupt requests. Two is using IEN and IRQ flags to decide which interrupt to be executed. Users have to check interrupt control bit and interrupt request flag in interrupt routine.

Ø Example: Check the interrupt request under multi-interrupt operation

```

                ORG            8                ; Interrupt vector
                JMP            INT_SERVICE
INT_SERVICE:
                ...                ; Push routine to save ACC and PFLAG to buffers.

INTP00CHK:
                B0BTS1        FP00IEN        ; Check INT0 interrupt request
                JMP            INTP01CHK      ; Check P00IEN
                B0BTS0        FP00IRQ        ; Jump check to next interrupt
                JMP            INTP00         ; Check P00IRQ
                B0BTS1        FP01IEN        ; Jump to INT0 interrupt service routine
                JMP            INTP01         ; Check INT0 interrupt request
                B0BTS0        FP01IRQ        ; Check P01IEN
                JMP            INTP01         ; Jump check to next interrupt
                B0BTS1        FT0IEN         ; Check P01IRQ
                JMP            INTT0CHK       ; Jump to INT1 interrupt service routine
                B0BTS0        FT0IRQ        ; Check T0 interrupt request
                JMP            INTT0         ; Check T0IEN
                B0BTS1        FTTC1IEN      ; Jump check to next interrupt
                JMP            INTTC1CHK     ; Check T0IRQ
                B0BTS0        FTTC1IRQ     ; Jump to T0 interrupt service routine
                JMP            INTT0         ; Check TC1 interrupt request
                B0BTS1        FTC1IEN       ; Check TC1IEN
                JMP            INT_EXIT      ; Jump to exit of IRQ
                B0BTS0        FTC1IRQ      ; Check TC1IRQ
                JMP            INTTC1       ; Jump to TC1 interrupt service routine
INT_EXIT:
                ...                ; Pop routine to load ACC and PFLAG from buffers.

                RETI                ; Exit interrupt vector

```

7 I/O PORT

7.1 I/O PORT MODE

The port direction is programmed by PnM register. All I/O ports can select input or output direction.

| 0B8H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P0M | P07M | P06M | P05M | P04M | P03M | P02M | P01M | P00M |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0C1H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P1M | P17M | P16M | P15M | P14M | P13M | P12M | P11M | P10M |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0C2H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P2M | P27M | P26M | P25M | P24M | P23M | P22M | P21M | P20M |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0C4H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P4M | - | P46M | P45M | P44M | P43M | P42M | P41M | P40M |
| Read/Write | - | R/W |
| After reset | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0C5H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P5M | P57M | P56M | P55M | P54M | P53M | P52M | P51M | P50M |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit[7:0] **PnM[7:0]**: Pn mode control bits. (n = 0~5).
 0 = Pn is input mode.
 1 = Pn is output mode.

Note:

1. Users can program them by bit control instructions (*B0BSET*, *B0BCLR*).
2. *P4.7* is input only pin, and the *P4M.7* keeps "1".

Ø Example: I/O mode selecting

```
CLR      P0M      ; Set all ports to be input mode.
CLR      P2M
CLR      P4M
CLR      P1M
CLR      P5M

MOV      A, #0FFH ; Set all ports to be output mode.
B0MOV   P0M, A
B0MOV   P1M, A
B0MOV   P2M,A
B0MOV   P4M,A
B0MOV   P5M, A

B0BCLR  P1M.2     ; Set P1.2 to be input mode.

B0BSET  P1M.2     ; Set P1.2 to be output mode.
```

7.2 I/O PULL UP REGISTER

| 0E0H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P0UR | P07R | P06R | P05R | P04R | P03R | P02R | P01R | P00R |
| Read/Write | W | W | W | W | W | W | W | W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0E1H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P1UR | P17R | P16R | P15R | P14R | P13R | P12R | P11R | P10R |
| Read/Write | W | W | W | W | W | W | W | W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0E2H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P2UR | P27R | P26R | P25R | P24R | P23R | P22R | P21R | P20R |
| Read/Write | W | W | W | W | W | W | W | W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0E4H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P4UR | - | P46R | P45R | P44R | P43R | P42R | P41R | P40R |
| Read/Write | - | W | W | W | W | W | W | W |
| After reset | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0E5H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P5UR | P57R | P56R | P55R | P54R | P53R | P52R | P51R | P50R |
| Read/Write | W | W | W | W | W | W | W | W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- **Note:** P4.7 is input only pin and without pull-up resistor. The P4UR.7 keeps "1".

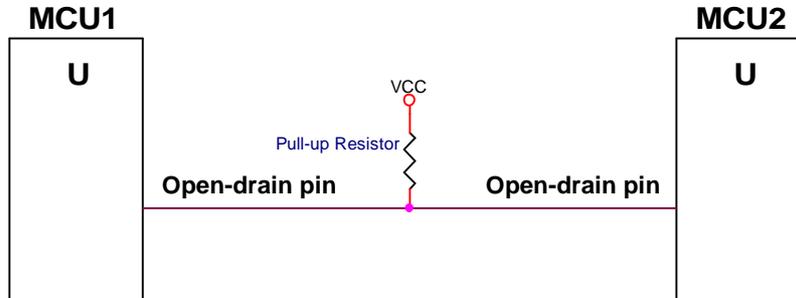
Ø Example: I/O Pull up Register

```

MOV      A, #0FFH      ; Enable Port0, 1, 2, 5 Pull-up register,
B0MOV    P0UR, A      ;
B0MOV    P1UR, A
B0MOV    P2UR,A
B0MOV    P4UR,A
B0MOV    P5UR, A
    
```

7.3 I/O OPEN-DRAIN REGISTER

P1.0, P1.1 are built-in open-drain function. P1.0, P1.1 must be set as output mode when enable open-drain function. Open-drain external circuit is as following.



The pull-up resistor is necessary. Open-drain output high is driven by pull-up resistor. Output low is sunken by MCU's pin.

| 0E9H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P10C | - | - | - | - | - | - | P110C | P100C |
| Read/Write | - | - | - | - | - | - | W | W |
| After reset | - | - | - | - | - | - | 0 | 0 |

Bit 0 **P100C:** P10 open-drain control bit
 0 = Disable open-drain mode
 1 = Enable open-drain mode

Bit 1 **P110C:** P11 open-drain control bit
 0 = Disable open-drain mode
 1 = Enable open-drain mode

Ø **Example: Enable P1.0 to open-drain mode and output high.**

```

B0BSET      P1.0           ; Set P1.0 buffer high.

B0BSET      P10M           ; Enable P1.0 output mode.
MOV         A, #01H       ; Enable P1.0 open-drain function.
B0MOV       P10C, A
    
```

- **Note: P10C is write only register. Setting P100C must be used "MOV" instructions.**

Ø **Example: Disable P1.0 to open-drain mode and output low.**

```

MOV         A, #0         ; Disable P1.0 open-drain function.
B0MOV       P10C, A
    
```

- **Note: After disable P1.0 open-drain function, P1.0 mode returns to last I/O mode.**

7.4 I/O PORT DATA REGISTER

| 0D0H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P0 | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0D1H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P1 | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0D2H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P2 | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0D4H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P4 | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 |
| Read/Write | R | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 0D5H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| P5 | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- **Note:** The P47 keeps "1" when external reset enable by code option.

∅ **Example: Read data from input port.**

```

B0MOV      A, P0           ; Read data from Port 0
B0MOV      A, P1           ; Read data from Port 1
B0MOV      A, P2           ; Read data from Port 2
B0MOV      A, P4           ; Read data from Port 4
B0MOV      A, P5           ; Read data from Port 5
    
```

∅ **Example: Write data to output port.**

```

MOV        A, #0FFH       ; Write data FFH to all Port.
B0MOV      P0, A
B0MOV      P1, A
B0MOV      P2, A
B0MOV      P4, A
B0MOV      P5, A
    
```

∅ **Example: Write one bit data to output port.**

```

B0BSET     P1.3           ; Set P1.3 and P5.5 to be "1".
B0BSET     P5.5

B0BCLR     P1.3           ; Set P1.3 and P5.5 to be "0".
B0BCLR     P5.5
    
```

8 TIMERS

8.1 WATCHDOG TIMER

The watchdog timer (WDT) is a binary up counter designed for monitoring program execution. If the program goes into the unknown status by noise interference, WDT overflow signal raises and resets MCU. Watchdog clock controlled by code option and the clock source is internal low-speed oscillator (16KHz @3V, 32KHz @5V).

Watchdog overflow time = 8192 / Internal Low-Speed oscillator (sec).

| VDD | Internal Low RC Freq. | Watchdog Overflow Time |
|-----|-----------------------|------------------------|
| 3V | 16KHz | 512ms |
| 5V | 32KHz | 256ms |

- **Note:**
1. If watchdog is "Always_On" mode, it keeps running event under power down mode or green mode.
 2. For S8KD ICE simulation, clear watchdog timer using "@RST_WDT" macro is necessary. Or the S8KD watchdog would be error.

Watchdog clear is controlled by WDTR register. Moving **0x5A** data into WDTR is to reset watchdog timer.

| OCCH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| WDTR | WDTR7 | WDTR6 | WDTR5 | WDTR4 | WDTR3 | WDTR2 | WDTR1 | WDTR0 |
| Read/Write | W | W | W | W | W | W | W | W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Ø **Example: An operation of watchdog timer is as following. To clear the watchdog timer counter in the top of the main routine of the program.**

Main:

```

MOV      A, #5AH           ; Clear the watchdog timer.
B0MOV    WDTR, A
...
...
CALL     SUB1
CALL     SUB2
...
...
JMP      MAIN

```

Ø **Example: Clear watchdog timer by @RST_WDT macro.**

```

Main:
        @RST_WDT                ; Clear the watchdog timer.
        ...
        ...
        CALL          SUB1
        CALL          SUB2
        ...
        ...
        JMP           MAIN

```

Watchdog timer application note is as following.

- I Before clearing watchdog timer, check I/O status and check RAM contents can improve system error.
- I Don't clear watchdog timer in interrupt vector and interrupt service routine. That can improve main routine fail.
- I Clearing watchdog timer program is only at one part of the program. This way is the best structure to enhance the watchdog timer function.

Example: An operation of watchdog timer is as following. To clear the watchdog timer counter in the top of the main routine of the program.

```

Main:
        ...                ; Check I/O.
        ...                ; Check RAM
Err:    JMP $              ; I/O or RAM error. Program jump here and don't
                                ; clear watchdog. Wait watchdog timer overflow to reset IC.

Correct:
        BOBSET          FWDRST ; I/O and RAM are correct. Clear watchdog timer and
                                ; execute program.
                                ; Only one clearing watchdog timer of whole program.
        ...
        CALL          SUB1
        CALL          SUB2
        ...
        ...
        JMP           MAIN

```

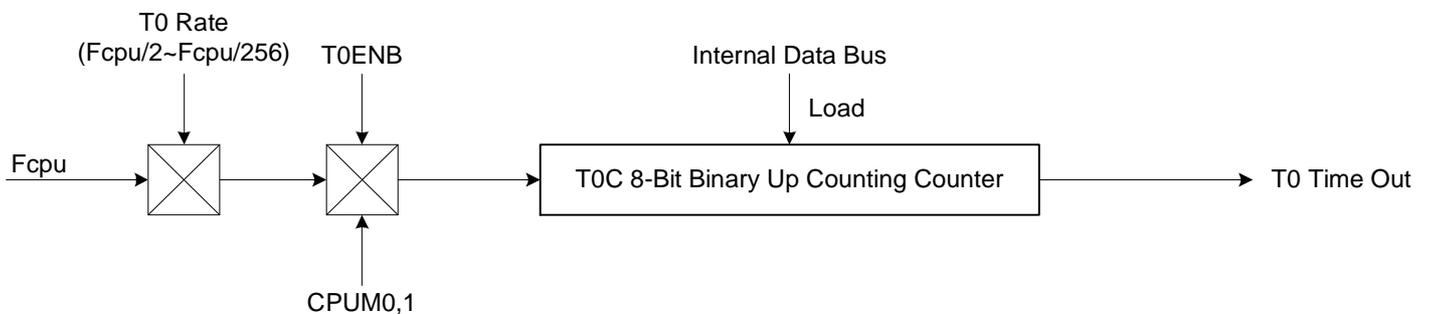
8.2 TIMER 0 (T0)

8.2.1 OVERVIEW

The T0 is an 8-bit binary up timer and event counter. If T0 timer occurs an overflow (from FFH to 00H), it will continue counting and issue a time-out signal to trigger T0 interrupt to request interrupt service.

The main purposes of the T0 timer is as following.

- F 8-bit programmable up counting timer:** Generates interrupts at specific time intervals based on the selected clock frequency.
- F Green mode wakeup function:** T0 can be green mode wake-up time as $T0ENB = 1$. System will be wake-up by T0 time out.



8.2.2 T0M MODE REGISTER

| 0D8H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|---------|---------|---------|-------|-------|-------|-------|
| T0M | TOENB | T0rate2 | T0rate1 | T0rate0 | - | - | - | - |
| Read/Write | R/W | R/W | R/W | R/W | - | - | - | - |
| After reset | 0 | 0 | 0 | 0 | - | - | - | - |

Bit [6:4] **TORATE[2:0]:** T0 internal clock select bits.

000 = fcpu/256.

001 = fcpu/128.

...

110 = fcpu/4.

111 = fcpu/2.

Bit 7 **TOENB:** T0 counter control bit.

0 = Disable T0 timer.

1 = Enable T0 timer.

8.2.3 T0C COUNTING REGISTER

T0C is an 8-bit counter register for T0 interval time control.

| | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0D9H | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| T0C | T0C7 | T0C6 | T0C5 | T0C4 | T0C3 | T0C2 | T0C1 | T0C0 |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The equation of T0C initial value is as following.

$$\text{T0C initial value} = 256 - (\text{T0 interrupt interval time} * \text{input clock})$$

Ø **Example:** To set 10ms interval time for T0 interrupt. High clock is external 4MHz. Fcpu=Fosc/4. Select TORATE=010 (Fcpu/64).

$$\begin{aligned} \text{T0C initial value} &= 256 - (\text{T0 interrupt interval time} * \text{input clock}) \\ &= 256 - (10\text{ms} * 4\text{MHz} / 4 / 64) \\ &= 256 - (10^{-2} * 4 * 10^6 / 4 / 64) \\ &= 100 \\ &= 64\text{H} \end{aligned}$$

The basic timer table interval time of T0.

| TORATE | T0CLOCK | High speed mode (Fcpu = 4MHz / 4) | | Low speed mode (Fcpu = 32768Hz / 4) | |
|--------|----------|-----------------------------------|--------------------|-------------------------------------|--------------------|
| | | Max overflow interval | One step = max/256 | Max overflow interval | One step = max/256 |
| 000 | Fcpu/256 | 65.536 ms | 256 us | 8000 ms | 31250 us |
| 001 | Fcpu/128 | 32.768 ms | 128 us | 4000 ms | 15625 us |
| 010 | Fcpu/64 | 16.384 ms | 64 us | 2000 ms | 7812.5 us |
| 011 | Fcpu/32 | 8.192 ms | 32 us | 1000 ms | 3906.25 us |
| 100 | Fcpu/16 | 4.096 ms | 16 us | 500 ms | 1953.125 us |
| 101 | Fcpu/8 | 2.048 ms | 8 us | 250 ms | 976.563 us |
| 110 | Fcpu/4 | 1.024 ms | 4 us | 125 ms | 488.281 us |
| 111 | Fcpu/2 | 0.512 ms | 2 us | 62.5 ms | 244.141 us |

- **Note:** T0C doesn't support read and modify write instructions as "B0ADD M,A . INCMS...".

8.2.4 T0 TIMER OPERATION SEQUENCE

T0 timer operation sequence of setup T0 timer is as following.

F Stop T0 timer counting, disable T0 interrupt function and clear T0 interrupt request flag.

```

B0BCLR    FT0ENB    ; T0 timer.
B0BCLR    FT0IEN    ; T0 interrupt function is disabled.
B0BCLR    FT0IRQ    ; T0 interrupt request flag is cleared.

```

F Set T0 timer rate.

```

MOV       A, #0xxx0000b    ;The T0 rate control bits exist in bit4~bit6 of T0M. The
                                ; value is from x000xxxxb~x111xxxxb.
B0MOV     T0M,A            ; T0 timer is disabled.

```

F Set T0 interrupt interval time.

```

MOV       A,#7FH
B0MOV     T0C,A            ; Set T0C value.

```

F Set T0 timer function mode.

```

B0BSET    FT0IEN    ; Enable T0 interrupt function.

```

F Enable T0 timer.

```

B0BSET    FT0ENB    ; Enable T0 timer.

```

8.2.5 T0 TIMER NOTICE

When T0C.7 is from "1" to "0", T0IRQ is set "1" whether T0 is operating or not. If T0IRQ = 0 and T0C is changed by program, T0IRQ might be set as T0C.7 is from "1" to "0". The condition makes unexpected T0 interrupt occurring.

Ø **Example: T0C = 0x80 (T0C.7 = 1) and T0IRQ = 0. T0IRQ will set as "1" when T0C is cleared by program (T0C.7 = 0).**

| | | |
|--------|--------|---|
| MOV | A, #0 | ; Clear T0C and T0C.7 is from "1" to "0". |
| B0MOV | T0C, A | ; T0IRQ changed from "0" to "1". |
| B0BSET | FT0IEN | ; Enable T0 interrupt function and system jumps to interrupt vector (ORG 8) at next cycle. |

If T0C changing in system operating duration is necessary, to disable T0 interrupt function (T0IEN = 0) before changing T0C value. The solution can avoid unexpected T0 interrupt occurring and example is as following.

Ø **Example: T0C = 0x80 and T0IRQ = 0. T0IRQ will change to "1" when T0C is cleared by program.**

| | | |
|--------|--------|---|
| B0BCLR | FT0IEN | ; Disable T0 interrupt function. |
| MOV | A, #0 | ; Clear T0C and T0C.7 is from "1" to "0". |
| B0MOV | T0C, A | ; T0IRQ changed from "0" to "1". |
| B0BCLR | FT0IRQ | ; Clear T0IRQ flag. |
| B0BSET | FT0IEN | ; Enable T0 interrupt function. |
| ... | | |
| ... | | |

- **Note: Disable T0 interrupt function first, and load new T0C value into T0C buffer. This way can avoid unexpected T0 interrupt occurring.**

- **Note: T0C doesn't support read and modify write instructions as "B0ADD M,A . INCMS...".**

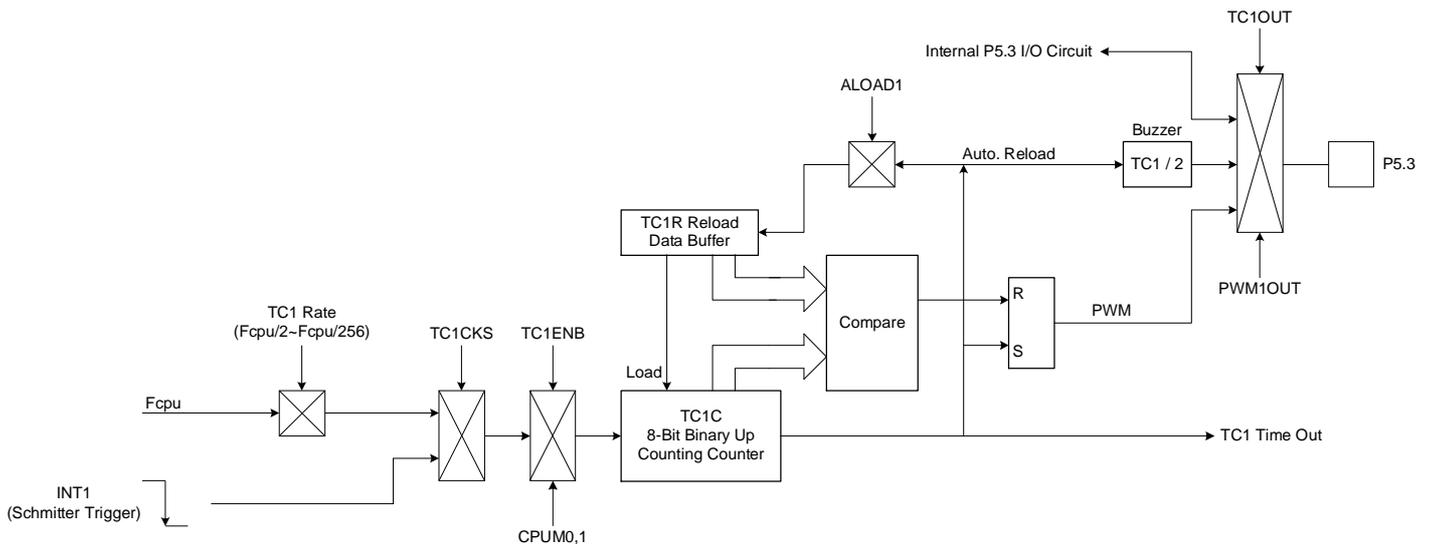
8.3 TIMER/COUNTER 1 (TC1)

8.3.1 OVERVIEW

The TC1 is an 8-bit binary up counting timer. TC1 has two clock sources including internal clock and external clock for counting a precision time. The internal clock source is from Fcpu. The external clock is INT1 from P0.1 pin (Falling edge trigger). Using TC1M register selects TC1C's clock source from internal or external. If TC1 timer occurs an overflow, it will continue counting and issue a time-out signal to trigger TC1 interrupt to request interrupt service. TC1 overflow time is 0xFF to 0X00 normally. Under PWM mode, TC1 overflow is still 256 counts.

The main purposes of the TC1 timer is as following.

- F 8-bit programmable up counting timer:** Generates interrupts at specific time intervals based on the selected clock frequency.
- F External event counter:** Counts system "events" based on falling edge detection of external clock signals at the INT1 input pin.
- F Buzzer output**
- F PWM output**



8.3.2 TC1M MODE REGISTER

| 0DCH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--------|----------|----------|----------|--------|--------|--------|---------|
| TC1M | TC1ENB | TC1rate2 | TC1rate1 | TC1rate0 | TC1CKS | ALOAD1 | TC1OUT | PWM1OUT |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- Bit 0 **PWM1OUT:** PWM output control bit.
0 = Disable PWM output.
1 = Enable PWM output. PWM duty controlled by TC1OUT, ALOAD1 bits.
- Bit 1 **TC1OUT:** TC1 time out toggle signal output control bit. **Only valid when PWM1OUT = 0.**
0 = Disable, P5.3 is I/O function.
1 = Enable, P5.3 is output TC1OUT signal.
- Bit 2 **ALOAD1:** Auto-reload control bit. **Only valid when PWM1OUT = 0.**
0 = Disable TC1 auto-reload function.
1 = Enable TC1 auto-reload function.
- Bit 3 **TC1CKS:** TC1 clock source select bit.
0 = Internal clock (Fcpu).
1 = External clock from P0.1/INT1 pin.
- Bit [6:4] **TC1RATE[2:0]:** TC1 internal clock select bits.
000 = fcpu/256.
001 = fcpu/128.
...
110 = fcpu/4.
111 = fcpu/2.
- Bit 7 **TC1ENB:** TC1 counter control bit.
0 = Disable TC1 timer.
1 = Enable TC1 timer.

- **Note: When TC1CKS=1, TC1 became an external event counter and TC1RATE is useless. No more P0.1 interrupt request will be raised. (P0.1IRQ will be always 0).**

8.3.3 TC1C COUNTING REGISTER

TC1C is an 8-bit counter register for TC1 interval time control.

| ODDH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| TC1C | TC1C7 | TC1C6 | TC1C5 | TC1C4 | TC1C3 | TC1C2 | TC1C1 | TC1C0 |
| Read/Write | R/W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The equation of TC1C initial value is as following.

| |
|---|
| $TC1C \text{ initial value} = 256 - (TC1 \text{ interrupt interval time} * \text{input clock})$ |
|---|

Ø **Example:** To set 10ms interval time for TC1 interrupt. TC1 clock source is Fcpu (TC1KS=0). High clock is external 4MHz. Fcpu=Fosc/4. Select TC1RATE=010 (Fcpu/64).

$$\begin{aligned}
 TC1C \text{ initial value} &= 256 - (TC1 \text{ interrupt interval time} * \text{input clock}) \\
 &= 256 - (10\text{ms} * 4\text{MHz} / 4 / 64) \\
 &= 256 - (10^{-2} * 4 * 10^6 / 4 / 64) \\
 &= 100 \\
 &= 64H
 \end{aligned}$$

The basic timer table interval time of TC1.

| TC1RATE | TC1CLOCK | High speed mode (Fcpu = 4MHz / 4) | | Low speed mode (Fcpu = 32768Hz / 4) | |
|---------|----------|-----------------------------------|--------------------|-------------------------------------|--------------------|
| | | Max overflow interval | One step = max/256 | Max overflow interval | One step = max/256 |
| 000 | Fcpu/256 | 65.536 ms | 256 us | 8000 ms | 31250 us |
| 001 | Fcpu/128 | 32.768 ms | 128 us | 4000 ms | 15625 us |
| 010 | Fcpu/64 | 16.384 ms | 64 us | 2000 ms | 7812.5 us |
| 011 | Fcpu/32 | 8.192 ms | 32 us | 1000 ms | 3906.25 us |
| 100 | Fcpu/16 | 4.096 ms | 16 us | 500 ms | 1953.125 us |
| 101 | Fcpu/8 | 2.048 ms | 8 us | 250 ms | 976.563 us |
| 110 | Fcpu/4 | 1.024 ms | 4 us | 125 ms | 488.281 us |
| 111 | Fcpu/2 | 0.512 ms | 2 us | 62.5 ms | 244.141 us |

8.3.4 TC1R AUTO-LOAD REGISTER

TC1 timer is with auto-load function controlled by ALOAD1 bit of TC1M. When TC1C overflow occurring, TC1R value will load to TC1C by system. It is easy to generate an accurate time, and users don't reset TC1C during interrupt service routine.

| ODEH | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| TC1R | TC1R7 | TC1R6 | TC1R5 | TC1R4 | TC1R3 | TC1R2 | TC1R1 | TC1R0 |
| Read/Write | W | W | W | W | W | W | W | W |
| After reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The equation of TC1R initial value is as following.

$$TC1R \text{ initial value} = N - (TC1 \text{ interrupt interval time} * \text{input clock})$$

N is TC1 overflow boundary number. TC1 timer overflow time has five types (TC1 timer, TC1 event counter, TC1 Fcpu clock source, PWM mode and no PWM mode). These parameters decide TC1 overflow time and valid value as follow table.

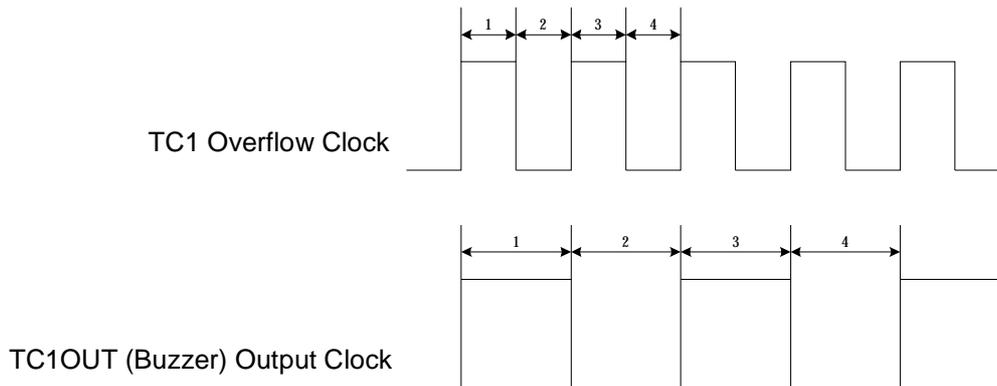
| TC1CKS | PWM1 | ALOAD1 | TC1OUT | N | TC1R valid value | TC1R value binary type |
|--------|------|--------|--------|-----|------------------|------------------------|
| 0 | 0 | x | x | 256 | 0x00~0xFF | 00000000b~11111111b |
| | 1 | 0 | 0 | 256 | 0x00~0xFF | 00000000b~11111111b |
| | 1 | 0 | 1 | 64 | 0x00~0x3F | xx000000b~xx111111b |
| | 1 | 1 | 0 | 32 | 0x00~0x1F | xxx00000b~xxx11111b |
| | 1 | 1 | 1 | 16 | 0x00~0x0F | xxxx0000b~xxxx1111b |
| 1 | - | - | - | 256 | 0x00~0xFF | 00000000b~11111111b |

Ø **Example:** To set 10ms interval time for TC1 interrupt. TC1 clock source is Fcpu (TC1KS=0) and no PWM output (PWM1=0). High clock is external 4MHz. Fcpu=Fosc/4. Select TC1RATE=010 (Fcpu/64).

$$\begin{aligned}
 TC1R \text{ initial value} &= N - (TC1 \text{ interrupt interval time} * \text{input clock}) \\
 &= 256 - (10ms * 4MHz / 4 / 64) \\
 &= 256 - (10^{-2} * 4 * 10^6 / 4 / 64) \\
 &= 100 \\
 &= 64H
 \end{aligned}$$

8.3.5 TC1 CLOCK FREQUENCY OUTPUT (BUZZER)

Buzzer output (TC1OUT) is from TC1 timer/counter frequency output function. By setting the TC1 clock frequency, the clock signal is output to P5.3 and the P5.3 general purpose I/O function is auto-disable. The TC1OUT frequency is divided by 2 from TC1 interval time. TC1OUT frequency is 1/2 TC1 frequency. The TC1 clock has many combinations and easily to make difference frequency. The TC1OUT frequency waveform is as following.



Ø **Example: Setup TC1OUT output from TC1 to TC1OUT (P5.3). The external high-speed clock is 4MHz. The TC1OUT frequency is 0.5KHz. Because the TC1OUT signal is divided by 2, set the TC1 clock to 1KHz. The TC1 clock source is from external oscillator clock. TC1 rate is $F_{cpu}/4$. The $TC1RATE2-TC1RATE1 = 110$. $TC1C = TC1R = 131$.**

```

MOV      A,#01100000B
BOBMV   TC1M,A           ; Set the TC1 rate to Fcpu/4

MOV      A,#131
BOBMV   TC1C,A          ; Set the auto-reload reference value
BOBMV   TC1R,A

BOBSET  FTC1OUT         ; Enable TC1 output to P5.3 and disable P5.3 I/O function
BOBSET  FALOAD1        ; Enable TC1 auto-reload function
BOBSET  FTC1ENB        ; Enable TC1 timer

```

- **Note: Buzzer output is enable, and "PWM1OUT" must be "0".**

8.3.6 TC1 TIMER OPERATION SEQUENCE

TC1 timer operation includes timer interrupt, event counter, TC1OUT and PWM. The sequence of setup TC1 timer is as following.

F Stop TC1 timer counting, disable TC1 interrupt function and clear TC1 interrupt request flag.

```
B0BCLR    FTC1ENB    ; TC1 timer, TC1OUT and PWM stop.
B0BCLR    FTC1IEN    ; TC1 interrupt function is disabled.
B0BCLR    FTC1IRQ    ; TC1 interrupt request flag is cleared.
```

F Set TC1 timer rate. (Besides event counter mode.)

```
MOV       A, #0xx0000b ;The TC1 rate control bits exist in bit4~bit6 of TC1M. The
                        ; value is from x000xxxxb~x111xxxxb.
B0MOV     TC1M,A       ; TC1 timer is disabled.
```

F Set TC1 timer clock source.

; Select TC1 internal / external clock source.

```
B0BCLR    FTC1CKS    ; Select TC1 internal clock source.
```

or

```
B0BSET    FTC1CKS    ; Select TC1 external clock source.
```

F Set TC1 timer auto-load mode.

```
B0BCLR    FALOAD1    ; Enable TC1 auto reload function.
```

or

```
B0BSET    FALOAD1    ; Disable TC1 auto reload function.
```

F Set TC1 interrupt interval time, TC1OUT (Buzzer) frequency or PWM duty cycle.

; Set TC1 interrupt interval time, TC1OUT (Buzzer) frequency or PWM duty.

```
MOV       A,#7FH      ; TC1C and TC1R value is decided by TC1 mode.
B0MOV     TC1C,A      ; Set TC1C value.
B0MOV     TC1R,A      ; Set TC1R value under auto reload mode or PWM mode.
```

; In PWM mode, set PWM cycle.

```
B0BCLR    FALOAD1    ; ALOAD1, TC1OUT = 00, PWM cycle boundary is 0~255.
B0BCLR    FTC1OUT
```

or

```
B0BCLR    FALOAD1    ; ALOAD1, TC1OUT = 01, PWM cycle boundary is 0~63.
B0BSET    FTC1OUT
```

or

```
B0BSET    FALOAD1    ; ALOAD1, TC1OUT = 10, PWM cycle boundary is 0~31.
B0BCLR    FTC1OUT
```

or

```
B0BSET    FALOAD1    ; ALOAD1, TC1OUT = 11, PWM cycle boundary is 0~15.
B0BSET    FTC1OUT
```

F Set TC1 timer function mode.

```

B0BSET    FTC1IEN    ; Enable TC1 interrupt function.
or
B0BSET    FTC1OUT    ; Enable TC1OUT (Buzzer) function.
or
B0BSET    FPWM1OUT   ; Enable PWM function.

```

F Enable TC1 timer.

```

B0BSET    FTC1ENB    ; Enable TC1 timer.

```

8.3.7 TC1 TIMER NOTICE

When TC1C value changes from "0xFF" to not "0xFF", TC1IRQ is set "1" whether TC1 is operating or not. If TC1IRQ = 0 and TC1C is changed by program, TC1IRQ might be set as TC1C is from "0xFF" to not "0xFF". The condition makes unexpected TC1 interrupt occurring.

∅ **Example: TC1C = 0xFF and TC1IRQ = 0. TC1IRQ will set as "1" when TC1C is cleared by program (TC1C = 0).**

```

MOV       A, #0        ; Clear TC1C.
B0MOV     TC1C, A      ; TC1IRQ changed from "0" to "1".

B0BSET    FTC1IEN     ; Enable TC1 interrupt function and system jumps to interrupt
                    ; vector (ORG 8) at next cycle.

```

If TC1C changing in system operating duration is necessary, to disable TC1 interrupt function (TC1IEN = 0) before changing TC1C value. The solution can avoid unexpected TC1 interrupt occurring and example is as following.

∅ **Example: TC1C = 0xFF and TC1IRQ = 0. Clearing TC1C must be after TC1 interrupt disable.**

```

B0BCLR    FTC1IEN     ; Disable TC1 interrupt function.

MOV       A, #0        ; Clear TC1C.
B0MOV     TC1C, A      ; TC1IRQ changed from "0" to "1".

B0BCLR    FTC1IRQ     ; Clear TC1IRQ flag.

B0BSET    FTC1IEN     ; Enable TC1 interrupt function.
...
...

```

- **Note: Disable TC1 interrupt function first, and load new TC1C value into TC1C buffer. This way can avoid unexpected TC1 interrupt occurring.**

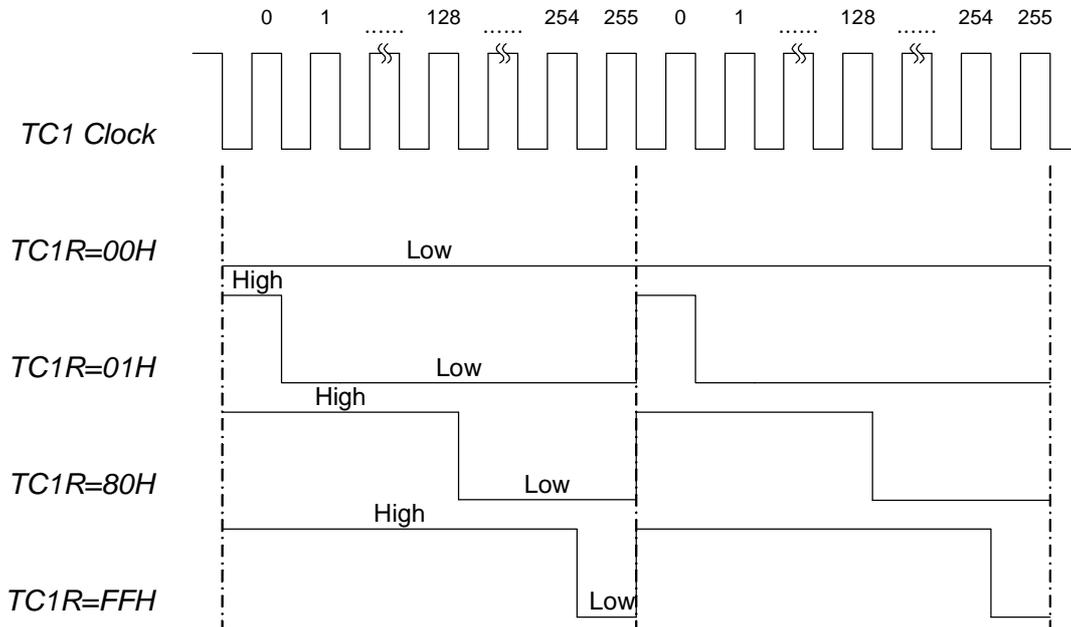
8.4 PWM1 MODE

8.4.1 OVERVIEW

PWM function is generated by TC1 timer counter and output the PWM signal to PWM1OUT pin (P5.3). The 8-bit counter counts modulus 256, 64, 32, 16 controlled by ALOAD1, TC1OUT bits. The value of the 8-bit counter (TC1C) is compared to the contents of the reference register (TC1R). When the reference register value (TC1R) is equal to the counter value (TC1C), the PWM output goes low. When the counter reaches zero, the PWM output is forced high. The low-to-high ratio (duty) of the PWM1 output is TC1R/256, 64, 32, 16.

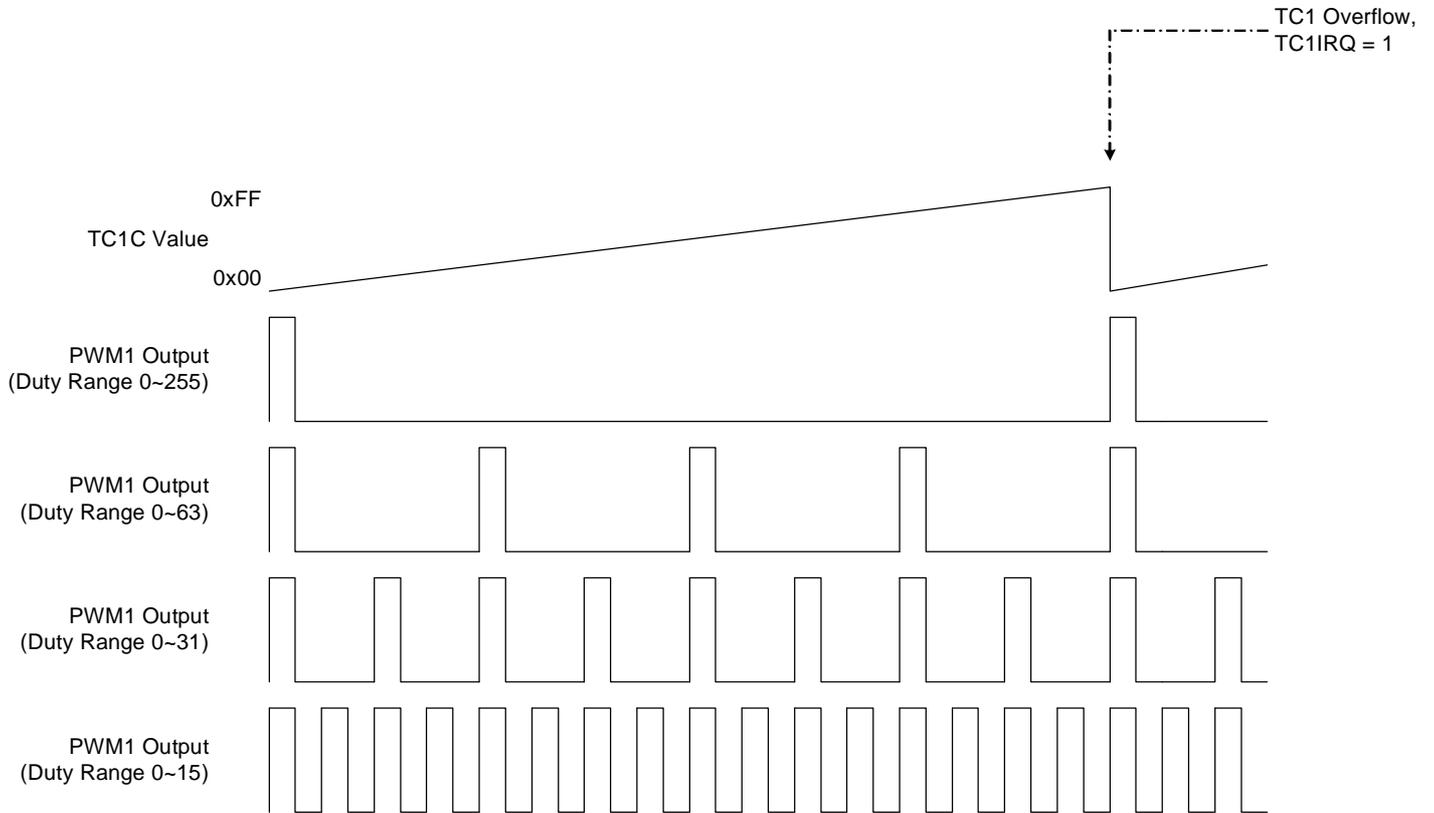
| ALOAD1 | TC1OUT | PWM duty range | TC1C valid value | TC1R valid bits value | MAX. PWM Frequency (Fcpu = 4MHz) | Remark |
|--------|--------|----------------|------------------|-----------------------|----------------------------------|------------------------|
| 0 | 0 | 0/256~255/256 | 0x00~0xFF | 0x00~0xFF | 7.8125K | Overflow per 256 count |
| 0 | 1 | 0/64~63/64 | 0x00~0x3F | 0x00~0x3F | 31.25K | Overflow per 64 count |
| 1 | 0 | 0/32~31/32 | 0x00~0x1F | 0x00~0x1F | 62.5K | Overflow per 32 count |
| 1 | 1 | 0/16~15/16 | 0x00~0x0F | 0x00~0x0F | 125K | Overflow per 16 count |

The Output duty of PWM is with different TC1R. Duty range is from 0/256~255/256.



8.4.2 TC1IRQ AND PWM DUTY

In PWM mode, the frequency of TC1IRQ is depended on PWM duty range. From following diagram, the TC1IRQ frequency is related with PWM duty.



8.4.3 PWM PROGRAM EXAMPLE

Example: Setup PWM1 output from TC1 to PWM1OUT (P5.3). The external high-speed oscillator clock is 4MHz. $F_{cpu} = F_{osc}/4$. The duty of PWM is 30/256. The PWM frequency is about 1KHz. The PWM clock source is from external oscillator clock. TC1 rate is $F_{cpu}/4$. The $TC1RATE2-TC1RATE1 = 110$. $TC1C = TC1R = 30$.

```

MOV      A,#01100000B
B0MOV   TC1M,A           ; Set the TC1 rate to Fcpu/4

MOV      A,#30
B0MOV   TC1C,A           ; Set the PWM duty to 30/256
B0MOV   TC1R,A

B0BCLR  FTC1OUT           ; Set duty range as 0/256~255/256.
B0BCLR  FALOAD1
B0BSET  FPWM1OUT          ; Enable PWM1 output to P5.3 and disable P5.3 I/O function
B0BSET  FTC1ENB           ; Enable TC1 timer

```

- **Note: The TC1R is write-only register. Don't process them using INCMS, DECMS instructions.**

Example: Modify TC1R registers' value.

```

MOV      A, #30H
B0MOV   TC1R, A           ; Input a number using B0MOV instruction.

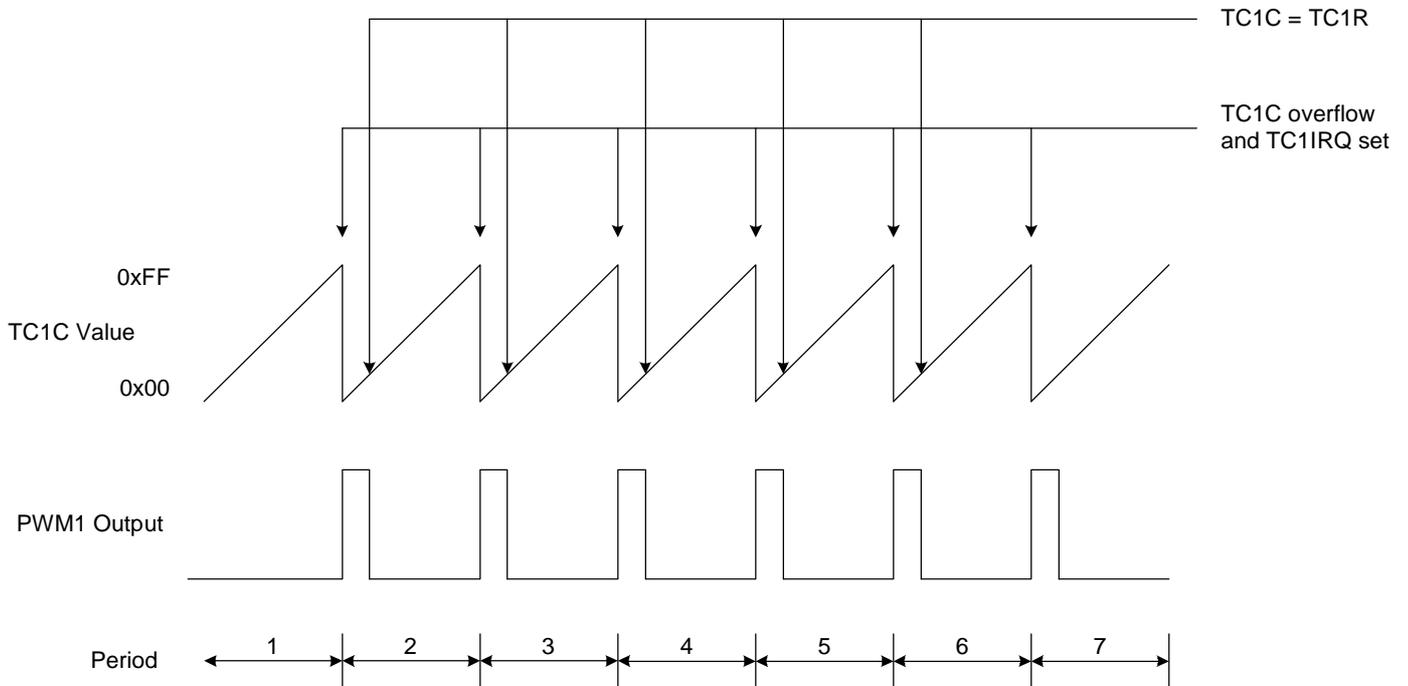
INCMS   BUF0              ; Get the new TC1R value from the BUF0 buffer defined by
NOP                                           ; programming.
B0MOV   A, BUF0
B0MOV   TC1R, A

```

- **Note: The PWM can work with interrupt request.**

8.4.4 PWM1 DUTY CHANGING NOTICE

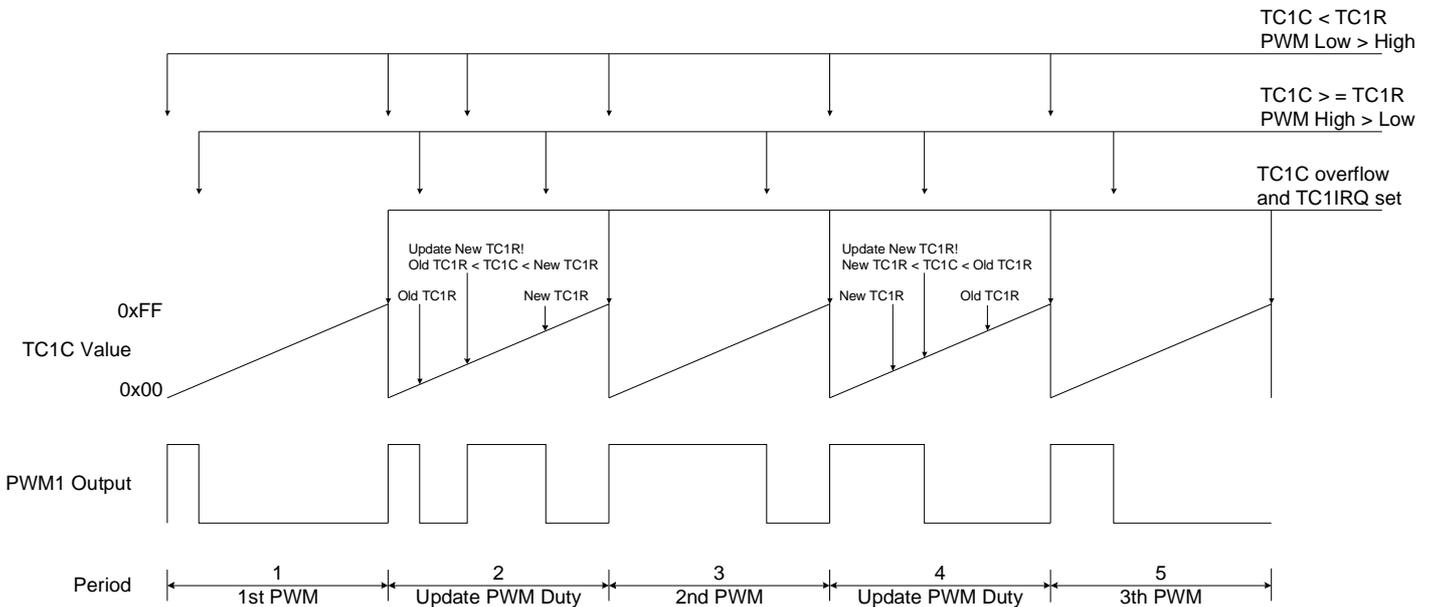
In PWM mode, the system will compare TC1C and TC1R all the time. When $TC1C < TC1R$, the PWM will output logic "High", when $TC1C \geq TC1R$, the PWM will output logic "Low". If TC1C is changed in certain period, the PWM duty will change immediately. If TC1R is fixed all the time, the PWM waveform is also the same.



Above diagram is shown the waveform with fixed TC1R. In every TC1C overflow PWM output "High, when $TC1C \geq TC1R$ PWM output "Low".

- **Note: Setting PWM duty in program processing must be at the new cycle start.**

If TC1R is changing in the program processing, the PWM waveform will become as following diagram.



In period 2 and period 4, new Duty (TC1R) is set, but the PWM output waveform of period 2 and period 4 are wrong. In period 2, the new TC1R value is greater than old TC1R value. If setting new TC1R is after PWM output “low”, system is getting TC1C < TC1R result and making PWM output “high”. There are two high level periods in the cycle, and the waveform is unexpected. Until next cycle, PWM outputs correct duty. In period 4, the new TC1R value is smaller than the old TC1R value. If setting new TC1R is before PWM output “low”, system is getting TC1C ≥ TC1R result and making PWM output “low”. In the cycle, the high duty is shorter than last cycle and longer than correct cycle. It is an unexpected PWM output.

Though the wrong waveforms only exist in one cycle, it is still a problem for precise PWM application and might make outside loading operations error. The solution is to load new TC1R after TC1 timer overflow. Using TC1IRQ status to determine TC1 timer is overflow or not. When TC1IRQ becomes “1”, to set the new TC1R value into TC1R buffer, and the unexpected PWM output is resolved.

Example: Using TC1 interrupt function to set new TC1R value for changing PWM duty.

MAIN:

```

...
B0MOV      TC1RBUF, A      ; Load new PWM duty setting value into TC1RBUF.
...
...

```

INT_SER:

```

...
...
; Push routine to save ACC and PFLAG to buffers.
...
B0BTS1    FTC1IRQ
JMP       INT_SER90
B0MOV     A, TC1RBUF      ; When TC1 Interrupt occurs, update TC1R.
B0MOV     TC1R, A
...
...

```

INT_SER90:

```

...
; Pop routine to load ACC and PFLAG from buffers.
RETI

```

9 INSTRUCTION TABLE

| Field | Mnemonic | Description | C | DC | Z | Cycle |
|---------|------------|--|--------------------------|----|---|-------|
| MOV | MOV A,M | $A \leftarrow M$ | - | - | √ | 1 |
| | MOV M,A | $M \leftarrow A$ | - | - | - | 1 |
| | B0MOV A,M | $A \leftarrow M$ (bank 0) | - | - | √ | 1 |
| | B0MOV M,A | M (bank 0) $\leftarrow A$ | - | - | - | 1 |
| | MOV A,I | $A \leftarrow I$ | - | - | - | 1 |
| | B0MOV M,I | $M \leftarrow I$, "M" only supports 0x80~0x87 registers (e.g. PFLAG,R,Y,Z...) | - | - | - | 1 |
| | XCH A,M | $A \leftrightarrow M$ | - | - | - | 1+N |
| | B0XCH A,M | $A \leftrightarrow M$ (bank 0) | - | - | - | 1+N |
| | MOVC | $R, A \leftarrow ROM [Y,Z]$ | - | - | - | 2 |
| ARITH | ADC A,M | $A \leftarrow A + M + C$, if occur carry, then $C=1$, else $C=0$ | √ | √ | √ | 1 |
| | ADC M,A | $M \leftarrow A + M + C$, if occur carry, then $C=1$, else $C=0$ | √ | √ | √ | 1+N |
| | ADD A,M | $A \leftarrow A + M$, if occur carry, then $C=1$, else $C=0$ | √ | √ | √ | 1 |
| | ADD M,A | $M \leftarrow A + M$, if occur carry, then $C=1$, else $C=0$ | √ | √ | √ | 1+N |
| | B0ADD M,A | M (bank 0) $\leftarrow M$ (bank 0) + A , if occur carry, then $C=1$, else $C=0$ | √ | √ | √ | 1+N |
| | ADD A,I | $A \leftarrow A + I$, if occur carry, then $C=1$, else $C=0$ | √ | √ | √ | 1 |
| | SBC A,M | $A \leftarrow A - M - /C$, if occur borrow, then $C=0$, else $C=1$ | √ | √ | √ | 1 |
| | SBC M,A | $M \leftarrow A - M - /C$, if occur borrow, then $C=0$, else $C=1$ | √ | √ | √ | 1+N |
| | SUB A,M | $A \leftarrow A - M$, if occur borrow, then $C=0$, else $C=1$ | √ | √ | √ | 1 |
| | SUB M,A | $M \leftarrow A - M$, if occur borrow, then $C=0$, else $C=1$ | √ | √ | √ | 1+N |
| | SUB A,I | $A \leftarrow A - I$, if occur borrow, then $C=0$, else $C=1$ | √ | √ | √ | 1 |
| | LOGIC | AND A,M | $A \leftarrow A$ and M | - | - | √ |
| AND M,A | | $M \leftarrow A$ and M | - | - | √ | 1+N |
| AND A,I | | $A \leftarrow A$ and I | - | - | √ | 1 |
| OR A,M | | $A \leftarrow A$ or M | - | - | √ | 1 |
| OR M,A | | $M \leftarrow A$ or M | - | - | √ | 1+N |
| OR A,I | | $A \leftarrow A$ or I | - | - | √ | 1 |
| XOR A,M | | $A \leftarrow A$ xor M | - | - | √ | 1 |
| XOR M,A | | $M \leftarrow A$ xor M | - | - | √ | 1+N |
| XOR A,I | | $A \leftarrow A$ xor I | - | - | √ | 1 |
| SHIFT | SWAP M | $A (b3-b0, b7-b4) \leftarrow M(b7-b4, b3-b0)$ | - | - | - | 1 |
| | SWAPM M | $M(b3-b0, b7-b4) \leftarrow M(b7-b4, b3-b0)$ | - | - | - | 1+N |
| | RRC M | $A \leftarrow RRC M$ | √ | - | - | 1 |
| | RRCM M | $M \leftarrow RRC M$ | √ | - | - | 1+N |
| | RLC M | $A \leftarrow RLC M$ | √ | - | - | 1 |
| | RLCM M | $M \leftarrow RLC M$ | √ | - | - | 1+N |
| | CLR M | $M \leftarrow 0$ | - | - | - | 1 |
| | BCLR M.b | $M.b \leftarrow 0$ | - | - | - | 1+N |
| | BSET M.b | $M.b \leftarrow 1$ | - | - | - | 1+N |
| | B0BCLR M.b | M (bank 0). $b \leftarrow 0$ | - | - | - | 1+N |
| | B0BSET M.b | M (bank 0). $b \leftarrow 1$ | - | - | - | 1+N |
| BRANCH | CMPRS A,I | $ZF,C \leftarrow A - I$, If $A = I$, then skip next instruction | √ | - | √ | 1 + S |
| | CMPRS A,M | $ZF,C \leftarrow A - M$, If $A = M$, then skip next instruction | √ | - | √ | 1 + S |
| | INCS M | $A \leftarrow M + 1$, If $A = 0$, then skip next instruction | - | - | - | 1 + S |
| | INCMS M | $M \leftarrow M + 1$, If $M = 0$, then skip next instruction | - | - | - | 1+N+S |
| | DECS M | $A \leftarrow M - 1$, If $A = 0$, then skip next instruction | - | - | - | 1 + S |
| | DECMS M | $M \leftarrow M - 1$, If $M = 0$, then skip next instruction | - | - | - | 1+N+S |
| | BTS0 M.b | If $M.b = 0$, then skip next instruction | - | - | - | 1 + S |
| | BTS1 M.b | If $M.b = 1$, then skip next instruction | - | - | - | 1 + S |
| | B0BTS0 M.b | If M (bank 0). $b = 0$, then skip next instruction | - | - | - | 1 + S |
| | B0BTS1 M.b | If M (bank 0). $b = 1$, then skip next instruction | - | - | - | 1 + S |
| | JMP d | $PC15/14 \leftarrow RomPages1/0, PC13-PC0 \leftarrow d$ | - | - | - | 2 |
| | CALL d | $Stack \leftarrow PC15-PC0, PC15/14 \leftarrow RomPages1/0, PC13-PC0 \leftarrow d$ | - | - | - | 2 |
| | MISC | RET | $PC \leftarrow Stack$ | - | - | - |
| NOP | | No operation | - | - | - | 1 |
| | | | | | | |

Note: 1. "M" is system register or RAM. If "M" is system registers then "N" = 0, otherwise "N" = 1.
 2. If branch condition is true then "S = 1", otherwise "S = 0".

10 ELECTRICAL CHARACTERISTIC

10.1 ABSOLUTE MAXIMUM RATING

| | |
|---|-------------------------|
| Supply voltage (Vdd)..... | - 0.3V ~ 6.0V |
| Input in voltage (Vin)..... | Vss – 0.2V ~ Vdd + 0.2V |
| Operating ambient temperature (Topr) | |
| SN8P2608P, SN8P2608X, SN8P2606P | 0°C ~ + 70°C |
| SN8P2608PD, SN8P2608XD, SN8P2606PD | -40°C ~ + 85°C |
| Storage ambient temperature (Tstor) | -40°C ~ + 125°C |

10.2 ELECTRICAL CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V, fosc = 4MHz, ambient temperature is 25°C unless otherwise note.)

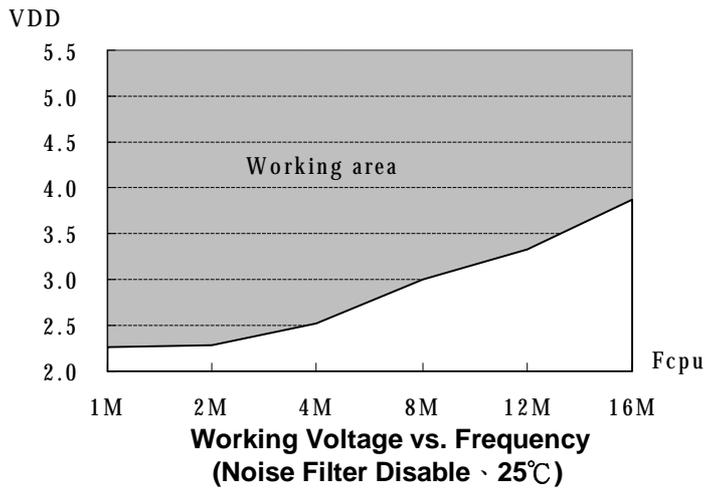
| PARAMETER | SYM. | DESCRIPTION | MIN. | TYP. | MAX. | UNIT | |
|---|------------------|---|----------------------|------|--------|-------|----|
| Operating voltage | Vdd | Normal mode, Vpp = Vdd, 25°C | 2.4 | 5.0 | 5.5 | V | |
| | | Normal mode, Vpp = Vdd, -40°C~85°C | 2.5 | 5.0 | 5.5 | V | |
| RAM Data Retention voltage | Vdr | | 1.5 | - | - | V | |
| Vdd rise rate | Vpor | Vdd rise rate to ensure internal power-on reset | 0.05 | - | - | V/ms | |
| Input Low Voltage | ViL1 | All input ports | Vss | - | 0.3Vdd | V | |
| | ViL2 | Reset pin | Vss | - | 0.2Vdd | V | |
| Input High Voltage | ViH1 | All input ports | 0.7Vdd | - | Vdd | V | |
| | ViH2 | Reset pin | 0.9Vdd | - | Vdd | V | |
| Reset pin leakage current | Ilekg | Vin = Vdd | - | - | 2 | uA | |
| I/O port pull-up resistor | Rup | Vin = Vss , Vdd = 3V | 100 | 200 | 300 | KΩ | |
| | | Vin = Vss , Vdd = 5V | 50 | 100 | 150 | | |
| I/O port input leakage current | Ilekg | Pull-up resistor disable, Vin = Vdd | - | - | 2 | uA | |
| I/O output source current sink current | IoH | Vop = Vdd – 0.5V | 8 | 12 | - | mA | |
| | IoL | Vop = Vss + 0.5V | 8 | 15 | - | | |
| INTn trigger pulse width | Tint0 | INT0 interrupt request pulse width | 2/fcpu | - | - | cycle | |
| Supply Current | Idd1 | normal Mode (No loading, Fcpu = Fosc/4) | Vdd= 5V, 4Mhz | - | 2.5 | 5 | mA |
| | | | Vdd= 3V, 4Mhz | - | 1 | 2 | mA |
| | Idd2 | Slow Mode (Internal low RC, Stop high clock) | Vdd= 5V, 32Khz | - | 25 | 50 | uA |
| | | | Vdd= 3V, 16Khz | - | 5 | 10 | uA |
| | Idd3 | Sleep Mode | Vdd= 5V, 25°C | - | 1 | 2 | uA |
| | | | Vdd= 3V , 25°C | - | 0.7 | 1.5 | uA |
| | | | Vdd= 5V, -40°C~85°C | - | 10 | 21 | uA |
| | | | Vdd= 3V , -40°C~85°C | - | 10 | 21 | uA |
| | Idd4 | Green Mode (No loading, Fcpu = Fosc/4, Watchdog Disable) | Vdd= 5V, 4Mhz | - | 0.50 | 1 | mA |
| | | | Vdd= 3V, 4Mhz | - | 0.20 | 0.4 | mA |
| Vdd=5V, ILRC 32Khz | | | - | 15 | 30 | uA | |
| Vdd=3V, ILRC 16Khz | | | - | 3 | 6 | uA | |
| LVD detect level | V _{LVD} | Low voltage detect level | 1.4 | 1.8 | 2.3 | V | |

*These parameters are for design reference, not tested.

10.3 CHARACTERISTIC GRAPHS

The Graphs in this section are for design guidance, not tested or guaranteed. In some graphs, the data presented are outside specified operating range. This is for information only and devices are guaranteed to operate properly only within the specified range.

SN8P2608



11 APPLICATION NOTICE

11.1 Development Tool Version

11.1.1 ICE (In circuit emulation)

- I **S8KD-2 ICE:** S8KD-2 ICE is designed for SN8P1XXX series emulation. There are some limitations if use S8KD-2 ICE emulates SN8P2608/SN8P2606 please refer following S8KD-2 ICE emulation notice section
- I **SN8ICE 2K:** Full function emulates SN8P2608/SN8P2606

11.1.2 OTP Writer

- I **Writer 3.0:** Support SN8P2608/SN8P2606 but no Stand-alone mode.
- I **Easy Writer V1.0:** OTP programming is controlled by ICE without firmware upgrade suffers. Please refer easy writer user manual for detailed information.
- I **MP-Easy Writer V1.0:** Stand-alone operation to support SN8P2608/SN8P2606 mass production

11.1.3 SN8IDE

SONiX 8-bit MCU integrated development environment include Assembler, ICE debugger and OTP writer software.

- I **For S8KD-2 ICE:** SN8IDE_V1.99R. **SN8IDE V1.99S or later No More support SN8P2000 series emulation.**
- I **For SN8ICE 2K:** M2IDE_V107 or later
- I **For Writer 3.0 and Easy Writer:** M2IDE_V107 or later

11.2 CODE OPTION

11.2.1 NOISE FILTER CODE OPTION

In high AC noisy environment should enable Noise_Filter code option. Enable Noise_Filter can reduce external noise affecting system of operating. **If Noise_Filter enable, the Fcpu is limited in “Fosc/4~Fosc/8”.**

| | Noise_Filter | |
|------|---------------|---------------|
| | Enable | Disable |
| Fcpu | Fosc/4~Fosc/8 | Fosc/1~Fosc/8 |

11.2.2 WATCHDOG

Watchdog of SN8P2608 includes three operations as Enable, Disable, Always On controlled by code option.

- Ø **Watchdog Enable:** If watchdog timer overflow during program running, the system resets. Watchdog timer stops in green mode and power down mode (sleep mode). After system wake-up, watchdog timer is running again.
- Ø **Watchdog Always On:** Watchdog timer keeps running in green mode or power down mode (sleep mode). If watchdog overflow occurs under the two modes, the system would be reset. It is not easy to make system to keep green mode/ power down mode situations. The main purpose of the design is supporting high AC noisy application. The watchdog timer guards system to work well and good reliability in high noisy situation.

11.3 INTERRUPT VECTOR (ORG 8)

When one of interrupt requests occurs, system will jump to interrupt vector and execute interrupt service routine. The first instruction of interrupt vector (ORG 8) must be "JMP" or "NOP". The SN8ASM199N and later version compilers alerts the message if the interrupt vector first instruction is not "JMP" or "NOP".

Ø **Example: The interrupt service routine is following ORG 8.**

```
.CODE
    ORG    0          ; 0000H
    JMP    START     ; Jump to user program address.
    ...

    ORG    8          ; Interrupt service routine
    NOP                    ; The first instruction at ORG 8.
    ...

    RETI                    ; End of interrupt service routine
    ...

START:
    ...                    ; The head of user program.
    ...                    ; User program
    JMP    START         ; End of user program
    ...

    ENDP                    ; End of program
```

Ø **Example: The interrupt service routine is following user program.**

```
.CODE
    ORG    0          ; 0000H
    JMP    START     ; Jump to user program address.
    ...

    ORG    08        ; 0008H, Jump to interrupt service routine address.
    JMP    MY_IRQ

START:
    ORG    10H       ; 0010H, The head of user program.
    ...              ; User program.
    ...
    JMP    START     ; End of user program.
    ...

MY_IRQ:
    ...              ; The head of interrupt service routine.
    ...
    RETI                    ; End of interrupt service routine.
    ...

    ENDP                    ; End of program.
```

11.4 S8KD-2 ICE ENULATION

SN8IDE is SONIX 8-bit development software including Assembler/ICE Debugger/OTP Writer. S8KD-2 is SONIX 8-bit ICE EV chip. There are different specifications between SN8P2608 and EV Chip. SONIX provides macros to solve the difference and make emulation correct. SN8IDE_V1.99R_S8KD2 and later version support these macros.

- **Note:**
1. *Please use SN8IDE V1.99R to develop projects!*
 2. *SN8IDE V1.99S or later No More support SN8P2000 series emulation.*

11.4.1 ICE_MODE

ICE_MODE setting is necessary. ICE_MODE = 1 supports S8KD-2 ICE emulation. ICE_MODE = 0 is real chip mode.

Syntax: ICE_MODE Val

Val: 0 = Real chip. 1 = S8KD-2 ICE emulation.

- Ø **Example: Setting ICE mode for ICE emulation. After compiling, the code only supports ICE emulation and can't work correct in real chip.**

```
CHIP          SN8P2608
.DATA

ICE_MODE     EQU          1          ; Set ICE_MODE for ICE emulation.

INCLUDESTD   SN8P2X_ICE.H

.CODE
User program
...
```

- Ø **Example: Setting ICE mode for real chip. After compiling, the code only supports SN8P2608 and can't work correct in ICE emulation.**

```
CHIP          SN8P2608
.DATA

ICE_MODE     EQU          0          ; Set ICE_MODE for real chip.

INCLUDESTD   SN8P2X_ICE.H

.CODE
User program
...
```

- **Note:**
1. *After ICE emulation and verifying all functions, set ICE_MODE = 0 and compile firmware again for real chip programming.*
 2. *Please use the ICE_MODE = 0 checksum for real chip code. Don't use ICE_MODE = 1 checksum which only support ICE emulation, not real chip.*

11.4.2 INSTRUCTION CYCLE

Instruction cycles of some instructions are different between SN8P2608/2606 and EV chip. These differences makes ICE instruction timing isn't consistent with SN8P2608/2606. SN8IDE assembler provides some macros to solve instruction cycle difference as following. Users just only use built-in instruction macro to replace corresponding instruction. In "ICE_MODE EQU 1" ICE emulation mode, assembler maybe insert some extra code to synchronize instruction timing between ICE and real chip. Therefore, the maximum available ROM size is larger than real chip. In "ICE_MODE EQU 0" the ROM size is same as real chip.

| SN8P2608 | | | | S8KD-2 EV CHIP | | | | INSTRUCTION MACRO | DESCRIPTION |
|--|----------|-------|-------|----------------|-------|-------|------------|---|-------------|
| Field | Mnemonic | Cycle | Field | Mnemonic | Cycle | | | | |
| M O V E | MOV | A,M | 1 | MOV | A,M | 1 | - | 1. M = RAM, N = 0. M = system register, N = 1. 2. S8KD-2 ICE : Read OSCM = 1 cycle Write OSCM = 2 cycle SN8P2608 : Read OSCM = 1 cycle Write OSCM = 1 cycle 3. PUSH,POP instructions are different between SN8P2608 and S8KD-2 ICE. | |
| | MOV | M,A | 1 | MOV | M,A | 1 | - | | |
| | B0MOV | A,M | 1 | B0MOV | A,M | 1 | - | | |
| | B0MOV | M,A | 1 | B0MOV | M,A | 1 | - | | |
| | MOV | A,I | 1 | MOV | A,I | 1 | - | | |
| | B0MOV | M,I | 1 | B0MOV | M,I | 1 | - | | |
| | XCH | A,M | 1+N | XCH | A,M | 1 | @XCH A,M | | |
| | B0XCH | A,M | 1+N | B0XCH | A,M | 1 | @B0XCH A,M | | |
| MOVC | | 2 | MOVC | | 2 | - | | | |
| A R I T H M E T I C | ADC | A,M | 1 | ADC | A,M | 1 | - | | |
| | ADC | M,A | 1+A | ADC | M,A | 1 | @ADC M,A | | |
| | ADD | A,M | 1 | ADD | A,M | 1 | - | | |
| | ADD | M,A | 1+N | ADD | M,A | 1 | @ADD M,A | | |
| | B0ADD | M,A | 1+N | B0ADD | M,A | 1 | @B0ADD M,A | | |
| | ADD | A,I | 1 | ADD | A,I | 1 | - | | |
| | SBC | A,M | 1 | SBC | A,M | 1 | - | | |
| | SBC | M,A | 1+N | SBC | M,A | 1 | @SBC M,A | | |
| L O G I C | AND | A,M | 1 | AND | A,M | 1 | - | | |
| | AND | M,A | 1+N | AND | M,A | 1 | @AND M,A | | |
| | AND | A,I | 1 | AND | A,I | 1 | - | | |
| | OR | A,M | 1 | OR | A,M | 1 | - | | |
| | OR | M,A | 1+N | OR | M,A | 1 | @OR M,A | | |
| | OR | A,I | 1 | OR | A,I | 1 | - | | |
| | XOR | A,M | 1 | XOR | A,M | 1 | - | | |
| | XOR | M,A | 1+N | XOR | M,A | 1 | @XOR M,A | | |
| P R O C E S S | SWAP | M | 1 | SWAP | M | 1 | - | | |
| | SWAPM | M | 1+N | SWAPM | M | 1 | @SWAPM M | | |
| | RRC | M | 1 | RRC | M | 1 | - | | |
| | RRCM | M | 1+N | RRCM | M | 1 | @RRCM M | | |
| | RLC | M | 1 | RLC | M | 1 | - | | |
| | RLCM | M | 1+N | RLCM | M | 1 | @RLCM M | | |
| | CLR | M | 1 | CLR | M | 1 | - | | |
| | BCLR | M.b | 1+N | BCLR | M.b | 1 | @BSET M.b | | |
| B R A N C H | CMPRS | A,I | 1 + S | CMPRS | A,I | 1 + S | - | | |
| | CMPRS | A,M | 1 + S | CMPRS | A,M | 1 + S | - | | |
| | INCS | M | 1 + S | INCS | M | 1 + S | - | | |
| | INCMS | M | 1+N+S | INCMS | M | 1 + S | @INCMS M | | |
| | DECS | M | 1 + S | DECS | M | 1 + S | - | | |
| | DECMS | M | 1+N+S | DECMS | M | 1 + S | @DECMS M | | |
| | BTS0 | M.b | 1 + S | BTS0 | M.b | 1 + S | - | | |
| | BTS1 | M.b | 1 + S | BTS1 | M.b | 1 + S | - | | |
| M I S C | B0BTS0 | M.b | 1 + S | B0BTS0 | M.b | 1 + S | - | | |
| | B0BTS1 | M.b | 1 + S | B0BTS1 | M.b | 1 + S | - | | |
| | JMP | d | 2 | JMP | d | 2 | - | | |
| | CALL | d | 2 | CALL | d | 2 | - | | |
| | RET | | 2 | RET | | 2 | - | | |
| | RETI | | 2 | RETI | | 2 | - | | |
| NOP | | 1 | NOP | | 1 | - | | | |
| PUSH | | 1 | PUSH | | 1 | - | | | |
| POP | | 1 | POP | | 1 | - | | | |

- **Note: S8KD-2 ICE can't emulate SN8P2608's "PUSH, POP" instructions.**

- **Note: The instruction macros of above table are built in "SN8P2X_ICE.H". The file must be included in user program.**

∅ **Example: Including SN8P2X_ICE.H in user program.**

```
CHIP          SN8P2608
.DATA
ICE_MODE     EQU          0

              INCLUDESTD  SN8P2X_ICE.H      ; SN8P2X_ICE.H is a standard macro file and included by
                                              "INCLUDESTD".

.CODE
              User program...
              ...
```

∅ **Example: Instructions are replaced by instruction macro.**

```
CHIP          SN8P2608
.DATA
ICE_MODE     EQU          0

              INCLUDESTD  SN8P2X_ICE.H

.CODE
              User program...

;             ADD          BUF1, A
              @ADD        BUF1, A          ; "ADD M,A" is replaced by "@ADD M,A".
              ...
;             AND          BUF1, A
              @AND        BUF1, A          ; "AND M,A" is replaced by "@AND M,A".
              ...
```

11.4.3 SYSTEM CLOCK

SONiX 2 series 8-bit MCU has multi-system clock ($F_{osc}/1 \sim F_{osc}/8, F_{osc}/64, F_{osc}/8,$), but ICE is fixed $F_{osc}/4$. In ICE emulation, user must be sure the F_{cpu} speeds of SN8P2608 and ICE are identical. Before emulation, change ICE crystal frequency to match with SN8P2608 system clock.

Ø Example: SN8P2608 system clock vs. ICE Table. The SN8P2608 clock source frequency is external 4MHz crystal.

| SN8P2604 Fcpu Option | Fcpu Frequency | ICE Fcpu | ICE Crystal Frequency |
|----------------------|----------------|-------------|-----------------------|
| $F_{osc}/1$ | 4MHz | $F_{osc}/4$ | 16MHz |
| $F_{osc}/2$ | 2MHz | $F_{osc}/4$ | 8MHz |
| $F_{osc}/4$ | 1MHz | $F_{osc}/4$ | 4MHz |
| $F_{osc}/8$ | 0.5MHz | $F_{osc}/4$ | 2MHz |

- **Note: For different speed crystals, modifying ICE "HIGH CLK" option is necessary. If ICE crystal is 16MHz, set "HIGH CLK" options to "X'TAL 12M".**

Ø Example: SN8P2608 system clock vs. ICE Table. The SN8P2608 clock source frequency is external 16MHz crystal.

| SN8P2604 Fcpu Option | Fcpu Frequency | ICE Fcpu | ICE Crystal Frequency |
|----------------------|----------------|-------------|-----------------------|
| $F_{osc}/1$ | 16MHz | $F_{osc}/4$ | - |
| $F_{osc}/2$ | 8MHz | $F_{osc}/4$ | - |
| $F_{osc}/4$ | 4MHz | $F_{osc}/4$ | 16MHz |
| $F_{osc}/8$ | 2MHz | $F_{osc}/4$ | 8MHz |

- **Note: ICE external high clock crystal is up to 16MHz. $F_{cpu} = F_{osc}/1$ and $F_{osc}/2$ can't be emulated. For the applications, users should use SN8P2608 to verify functions.**

11.4.4 WATCHDOG TIMER

Watchdog timer clear routine of SN8P2608 is setting WDTR register 0x5A. S8KD-2 ICE is not. SN8IDE provides “@RST_WDT” macro to make watchdog timer function correctly.

Ø **Example: Reset watchdog timer by setting WDTR as 0x5A.**

```
CHIP          SN8P2608
.DATA
ICE_MODE     EQU          0

              INCLUDESTD  SN8P2X_ICE.H

.CODE
              User program...

              MOV          A, #5Ah          ; Reset watchdog timer.
              B0MOV       WDTR, A

              ...
```

- **Note: This way can't be emulated in S8KD-2 ICE. Using following routine to replace it.**

Ø **Example: Reset watchdog timer by “@RST_WDT”.**

```
CHIP          SN8P2608
.DATA
ICE_MODE     EQU          0

              INCLUDESTD  SN8P2X_ICE.H

.CODE
              User program...

              @RST_WDT          ; Reset watchdog timer by macro.

              ...
```

11.4.5 P0 EMULATION

SN8P2608's P0 is bi-direction I/O, but ICE's P0 is input only. PEDGE controls are different, too. SN8IDE provides macros to control P0 emulation. These macros are built in assembler software.

11.4.5.1 @P0n_MODE

Syntax: @P0n_MODE Val (n = 0~7)

Val: 0 = Set P0.n input mode. 1 = Set P0.n output mode.

Ø Example: Set P0.0 as input mode.

```
@P00_MODE 0
```

- *Note: If P0 set as input mode, the input pins are P0.0~P0.7 of S8KD-2 ICE.*

Ø Example: Set P0.0 as output mode.

```
@P00_MODE 1
```

- *Note: If P0 set as output mode, the output pins are P6.0~P6.7 of S8KD-2 ICE.*

11.4.5.2 @P0n_OUT

Syntax: @P0n0_OUT Val (n = 0~7)

Val: 0 = Set P0.n0 output low. 1 = Set P0.n output high.

Ø Example: Set P0.0 as output high.

```
@P00_OUT 1
```

- *Note: Under P0 output mode, the signals are output from P6.0~P6.7 of S8KD-2 ICE.*

11.4.5.3 PEDGE

P00G[1:0] of PEDGE register definition is different from S8KD-2 ICE. ICE emulation and real chip PEDGE function are different.

| PEDGE | | SN8P2608 | S8KD-2 ICE |
|-------|-------|--------------|--------------|
| P00G1 | P00G0 | | |
| 0 | 0 | Reserved | Reserved |
| 0 | 1 | Rising Edge | Falling Edge |
| 1 | 0 | Falling Edge | Rising Edge |
| 1 | 1 | Bi-Direction | Bi-Direction |

SONiX provides “@P00_EDGE” macro to emulate real chip PEDGE function in ICE. The ICE_MODE must be 1 for ICE Emulation. After ICE emulation, set ICE_MODE as 0 and compile again to get SN8 file for real chip.

Syntax: @P00_EDGE Val

Val: 1 = Rising edge. 2 = Falling edge. 3 = Level change (bi-direction).

Ø **Example: Set P0.0 interrupt trigger as rising edge and ICE emulation.**

```
CHIP          SN8P2608
.DATA
ICE_MODE     EQU          1          ; Set ICE mode.

INCLUDESTD   SN8P2X_ICE.H

.CODE
User program...

@P00_EDGE 1          ; Set P0.0 interrupt trigger as rising edge.
BOBSET      FP00IEN
...
```

Ø **Example: Set P0.0 interrupt trigger as falling edge and for real chip “SN8”.**

```
CHIP          SN8P2608
.DATA
ICE_MODE     EQU          0          ; Set real chip mode.

INCLUDESTD   SN8P2X_ICE.H

.CODE
User program...

@P00_EDGE 2          ; Set P0.0 interrupt trigger as falling edge.
BOBSET      FP00IEN
...
```

11.4.6 PWM DUTY

PWM duty of SN8P2608 is controlled by ALOAD1, TC1OUT bits.

| PWM1OUT = 1 | | | | | |
|-------------|--------|---------------|-----------------|-------------------------------|------------------------|
| ALOAD1 | TC1OUT | TC1R Boundary | PWM duty range | Max PWM Frequency (Fcpu = 4M) | Note |
| 0 | 0 | 00h to FFh | 0/256 ~ 255/256 | 7.8125K | Overflow per 256 count |
| 0 | 1 | 00h to 3Fh | 0/64 ~ 63/64 | 31.25K | Overflow per 64 count |
| 1 | 0 | 00h to 1Fh | 0/32 ~ 31/32 | 62.5K | Overflow per 32 count |
| 1 | 1 | 00h to 0Fh | 0/16 ~ 15/16 | 125K | Overflow per 16 count |

S8KD-2 ICE doesn't support PWM duty setting function. SONiX provides PWM Duty setting macro. Users can use it to emulate PWM function and don't affect other functions. The macro is built in assembler software. Users have to set ICE_MODE as ICE or real chip.

Syntax: @PWM1_MAX_DUTY Max_Duty

| Max_Duty | TC1 Overflow Boundary | PWM Duty Range | PWM Resolution |
|----------|-----------------------|-----------------|----------------|
| 256 | FFh to 00h | 0/256 ~ 255/256 | 8-bit |
| 64 | 3Fh to 40h | 0/64 ~ 63/64 | 6-bit |
| 32 | 1Fh to 20h | 0/32 ~ 31/32 | 5-bit |
| 16 | 0Fh to 10h | 0/16 ~ 15/16 | 4-bit |

Ø **Example: Set PWM Max. Duty = 64, Duty = 2:1.**

```

CHIP          SN8P2608
.DATA
ICE_MODE     EQU          0          ; Set real chip mode.

INCLUDESTD   SN8P2X_ICE.H

.CODE
User program...

@PWM1_MAX_DUTY    64          ; Set PWM1 max. duty as 64.

MOV          A,#42          ; 42 = 63 (Max. TC1R) / 3 X 2
BOMOV       TC1R,A
BOBSET      FPWM1OUT
BOBSET      FTC1ENB
...

```

11.4.7 OTHER MACRO

A macro routine includes many instructions. It will be error after test instruction with skipping function.

```

        BTS0          BUF.0
        @RST_WDT
        JMP          TEST_CODE
TEST_CODE:
        ...

```

BTS0 instruction skipping function only skip one instruction. @RST_WDT is a macro and composed of several instructions. The skipping function of above routine would be error. It can't skip to "JMP TEST_CODE" successfully. Using following routines can solve the problem.

```

        BTS0          BUF.0
        JMP          CLR_WDT
        JMP          TEST_CODE
        ...
CLR_WDT:
        @RST_WDT
        ...
TEST_CODE:
        ...

```

SN8IDE provides user defined forward/backward jump directive to processing skipping function easier. "Macro_Start" and "Macro_End" is user define label name. Using @@.Macro_Start and @@.Macro_End to syntax. These label names can be repeated in main program.

```

        BTS0          BUF.0
        JMP          @@F.Macro_Start ; Jump to nearest user define @@.Macro_Start:
        JMP          @@F.Macro_End   ; Jump to nearest user define @@.Macro_End:
        ...

@@.Macro_Start:
        @RST_WDT
@@.Macro_End:

TEST_CODE:
        ...

```

- **Note: Only S8ASM V1.99N or later version support user defined forward/backward jump directive!**

- **Note: Macro possible affects Accumulator and PFLAG result. Users have to check it!**

12 OTP PROGRAMMING PIN

12.1.1 The pin assignment of Easy Writer transition board socket:

Easy Writer JP1/JP2

| | | | |
|-------------|----|----|------------|
| VSS | 2 | 1 | VDD |
| CE | 4 | 3 | CLK/PGCLK |
| OE/ShiftDat | 6 | 5 | PGM/OTPCLK |
| D0 | 8 | 7 | D1 |
| D2 | 10 | 9 | D3 |
| D4 | 12 | 11 | D5 |
| D6 | 14 | 13 | D7 |
| VPP | 16 | 15 | VDD |
| RST | 18 | 17 | HLS |
| ALSB/PDB | 20 | 19 | - |

JP1 for MP transition board

JP2 for Writer V3.0 transition board

Easy Writer JP3 (Mapping to 48-pin text tool)

| | | | |
|-------|----|----|-------|
| DIP1 | 1 | 48 | DIP48 |
| DIP2 | 2 | 47 | DIP47 |
| DIP3 | 3 | 46 | DIP46 |
| DIP4 | 4 | 45 | DIP45 |
| DIP5 | 5 | 44 | DIP44 |
| DIP6 | 6 | 43 | DIP43 |
| DIP7 | 7 | 42 | DIP42 |
| DIP8 | 8 | 41 | DIP41 |
| DIP9 | 9 | 40 | DIP40 |
| DIP10 | 10 | 39 | DIP39 |
| DIP11 | 11 | 38 | DIP38 |
| DIP12 | 12 | 37 | DIP38 |
| DIP13 | 13 | 36 | DIP36 |
| DIP14 | 14 | 35 | DIP35 |
| DIP15 | 15 | 34 | DIP34 |
| DIP16 | 16 | 33 | DIP33 |
| DIP17 | 17 | 32 | DIP32 |
| DIP18 | 18 | 31 | DIP31 |
| DIP19 | 19 | 30 | DIP30 |
| DIP20 | 20 | 29 | DIP29 |
| DIP21 | 21 | 28 | DIP28 |
| DIP22 | 22 | 27 | DIP27 |
| DIP23 | 23 | 26 | DIP26 |
| DIP24 | 24 | 25 | DIP25 |

JP3 for MP transition board

12.1.2 The pin assignment of Writer V3.0 and V2.5 transition board socket:

| | | | |
|-----|----|----|-----|
| GND | 1 | 2 | VDD |
| CE | 3 | 4 | CLK |
| OE | 5 | 6 | PGM |
| D0 | 7 | 8 | D1 |
| D2 | 9 | 10 | D3 |
| D4 | 11 | 12 | D5 |
| D6 | 13 | 14 | D7 |
| VPP | 15 | 16 | VDD |
| RST | 17 | 18 | HLS |

Writer V2.5 JP1 Pin Assignment

| | | | |
|-----|----|----|-----|
| GND | 2 | 1 | VDD |
| CE | 4 | 3 | CLK |
| OE | 6 | 5 | PGM |
| D0 | 8 | 7 | D1 |
| D2 | 10 | 9 | D3 |
| D4 | 12 | 11 | D5 |
| D6 | 14 | 13 | D7 |
| VPP | 16 | 15 | VDD |
| RST | 18 | 17 | HLS |
| | 20 | 19 | |

Writer V3.0 JP1 Pin Assignment

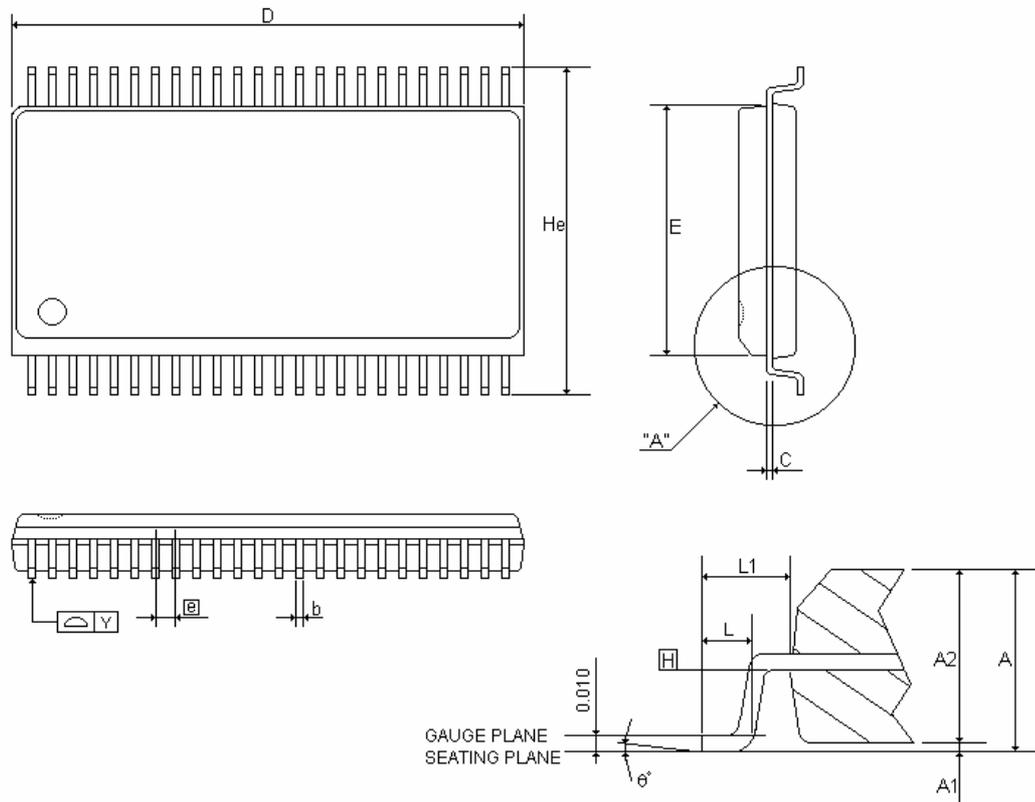
Note: For supporting the body programming, SONiX writer V2.5 must update V3.0 firmware and modify circuit. Please contact SONiX agent about SONiX Writer V2.5 upgrade.

12.1.3 SN8P2608/SN8P2606 Programming Pin Mapping:

| Programming Information of SN8P2600A Series | | | | | | | | | | | |
|---|------|-----------------------------------|----------|----------------------------|------|----------|------|--|--|--|--|
| Chip Name | | | | SN8P2606 | | SN8P2608 | | | | | |
| Writer V2.5 Connector | | EZ Writer / Writer V3.0 Connector | | OTP IC / JP3 Pin Assigment | | | | | | | |
| Number | Name | Number | Name | Number | Pin | Number | Pin | | | | |
| 2 | VDD | 1 | VDD | 11,32 | VDD | 13,39 | VDD | | | | |
| 1 | GND | 2 | GND | 12,31 | VSS | 14,36 | VSS | | | | |
| 4 | CLK | 3 | CLK | 21 | P5.0 | 25 | P5.0 | | | | |
| 3 | CE | 4 | CE | - | - | - | - | | | | |
| 6 | PGM | 5 | PGM | 40 | P1.0 | 1 | P1.0 | | | | |
| 5 | OE | 6 | OE | 20 | P5.1 | 24 | P5.1 | | | | |
| 8 | D1 | 7 | D1 | - | - | - | - | | | | |
| 7 | D0 | 8 | D0 | - | - | - | - | | | | |
| 10 | D3 | 9 | D3 | - | - | - | - | | | | |
| 9 | D2 | 10 | D2 | - | - | - | - | | | | |
| 12 | D5 | 11 | D5 | - | - | - | - | | | | |
| 11 | D4 | 12 | D4 | - | - | - | - | | | | |
| 14 | D7 | 13 | D7 | - | - | - | - | | | | |
| 13 | D6 | 14 | D6 | - | - | - | - | | | | |
| 16 | VDD | 15 | VDD | - | - | - | - | | | | |
| 15 | VPP | 16 | VPP | 1 | RST | 2 | RST | | | | |
| 18 | HLS | 17 | HLS | - | - | - | - | | | | |
| 17 | RST | 18 | RST | - | - | - | - | | | | |
| - | - | 19 | - | - | - | - | - | | | | |
| - | - | 20 | ALSB/PDB | 2 | P1.1 | 3 | P1.1 | | | | |

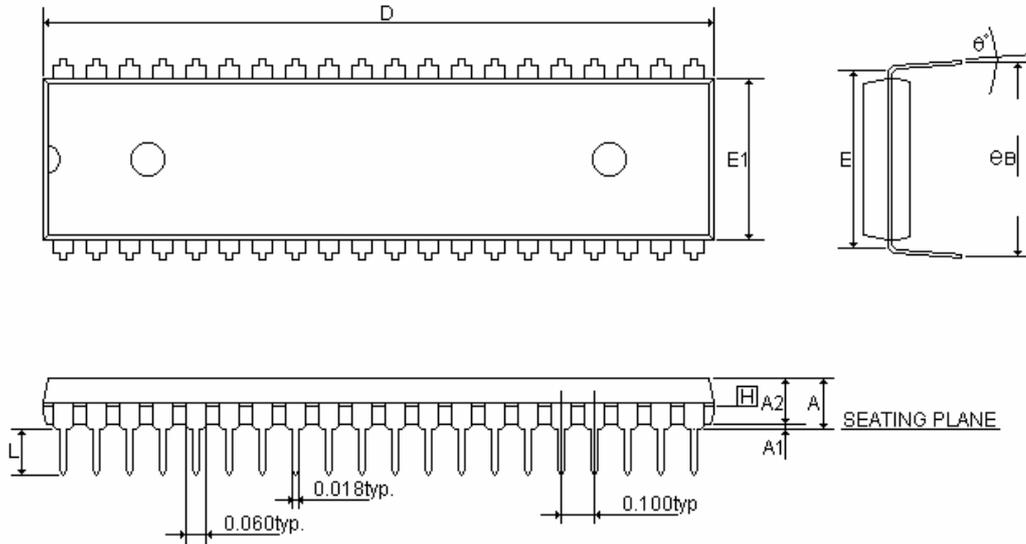
13 PACKAGE INFORMATION

13.1 SSOP 48 PIN



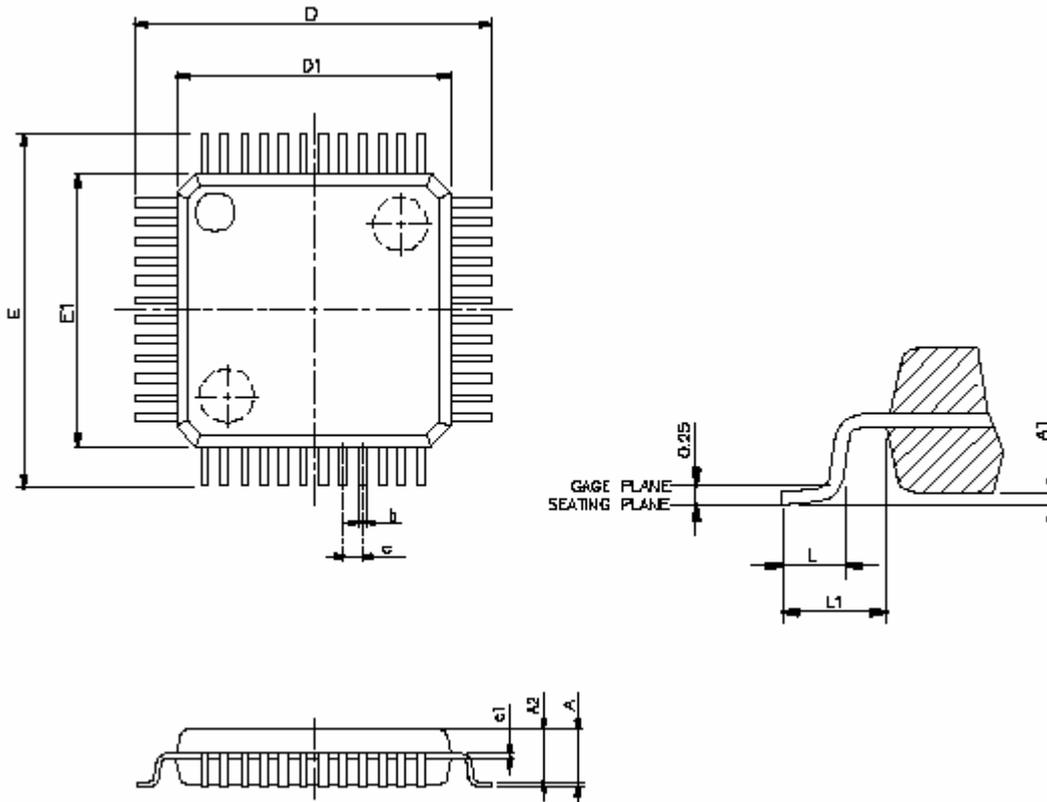
| SYMBOLS | MIN | NOR | MAX | MIN | NOR | MAX |
|----------------|--------|-------|-------|--------|--------|--------|
| | (inch) | | | (mm) | | |
| A | 0.095 | 0.102 | 0.110 | 2.413 | 2.591 | 2.794 |
| A1 | 0.008 | 0.012 | 0.016 | 0.203 | 0.305 | 0.406 |
| A2 | 0.089 | 0.094 | 0.099 | 2.261 | 2.388 | 2.515 |
| b | 0.008 | 0.010 | 0.030 | 0.203 | 0.254 | 0.762 |
| C | - | 0.008 | - | - | 0.203 | - |
| D | 0.620 | 0.625 | 0.630 | 15.748 | 15.875 | 16.002 |
| E | 0.291 | 0.295 | 0.299 | 7.391 | 7.493 | 7.595 |
| [e] | - | 0.025 | - | - | 0.635 | - |
| He | 0.396 | 0.406 | 0.416 | 10.058 | 10.312 | 10.566 |
| L | 0.020 | 0.030 | 0.040 | 0.508 | 0.762 | 1.016 |
| L1 | - | 0.056 | - | - | 1.422 | - |
| Y | - | - | 0.003 | - | - | 0.076 |
| θ° | 0° | - | 8° | 0° | - | 8° |

13.2 P-DIP 40 PIN



| SYMBOLS | MIN | NOR | MAX | MIN | NOR | MAX |
|---------|--------|-------|-------|--------|--------|--------|
| | (inch) | | | (mm) | | |
| A | - | - | 0.220 | - | - | 5.588 |
| A1 | 0.015 | - | - | 0.381 | - | - |
| A2 | 0.150 | 0.115 | 0.160 | 3.810 | 2.921 | 4.064 |
| D | 2.055 | 2.060 | 2.070 | 52.197 | 52.324 | 52.578 |
| E | 0.600 | | | 15.240 | | |
| E1 | 0.540 | 0.545 | 0.550 | 13.716 | 13.843 | 13.970 |
| L | 0.115 | 0.130 | 0.150 | 2.921 | 3.302 | 3.810 |
| eB | 0.630 | 0.650 | 0.067 | 16.002 | 16.510 | 1.702 |
| θ° | 0° | 7° | 15° | 0° | 7° | 15° |

13.3 LQFP 48 PIN



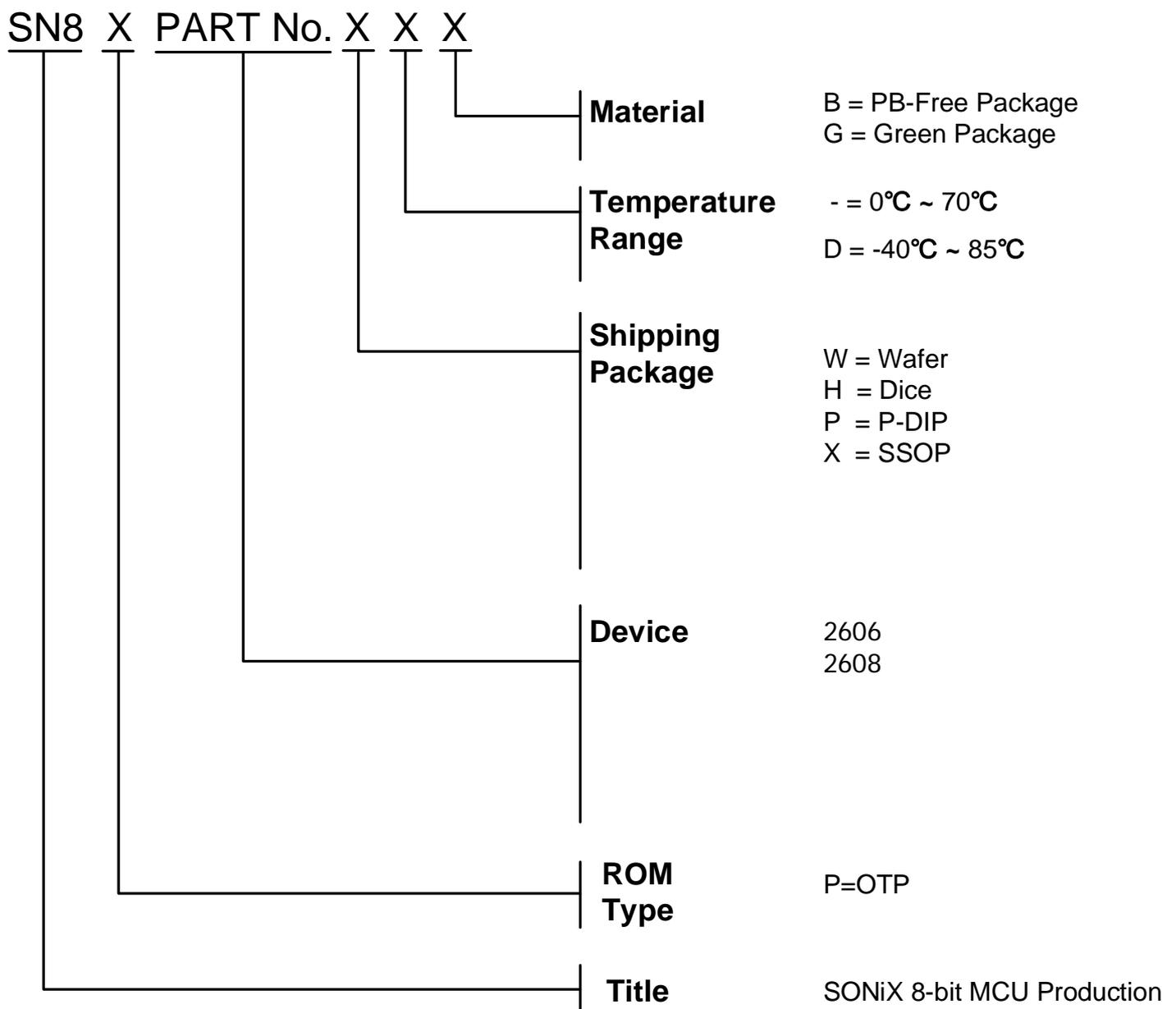
| SYMBOLS | MIN | NOR | MAX | MIN | NOR | MAX |
|---------|-----------|-----|-------|----------|-----|------|
| | (inch) | | | (mm) | | |
| A | - | - | 0.063 | - | - | 1.6 |
| A1 | 0.002 | - | 0.006 | 0.05 | - | 0.15 |
| A2 | 0.053 | - | 0.057 | 1.35 | - | 1.45 |
| c1 | 0.004 | - | 0.006 | 0.09 | - | 0.16 |
| D | 0.354 BSC | | | 9.00 BSC | | |
| D1 | 0.276 BSC | | | 7.00 BSC | | |
| E | 0.354 BSC | | | 9.00 BSC | | |
| E1 | 0.276 BSC | | | 7.00 BSC | | |
| e | 0.020 BSC | | | 0.5 BSC | | |
| B | 0.007 | - | 0.011 | 0.17 | - | 0.27 |
| L | 0.018 | - | 0.030 | 0.45 | - | 0.75 |
| L1 | 0.039 REF | | | 1 REF | | |

14 Marking Definition

14.1 INTRODUCTION

There are many different types in Sonix 8-bit MCU production line. This note listed the production definition of all 8-bit MCU for order or obtain information. This definition is only for Blank OTP MCU.

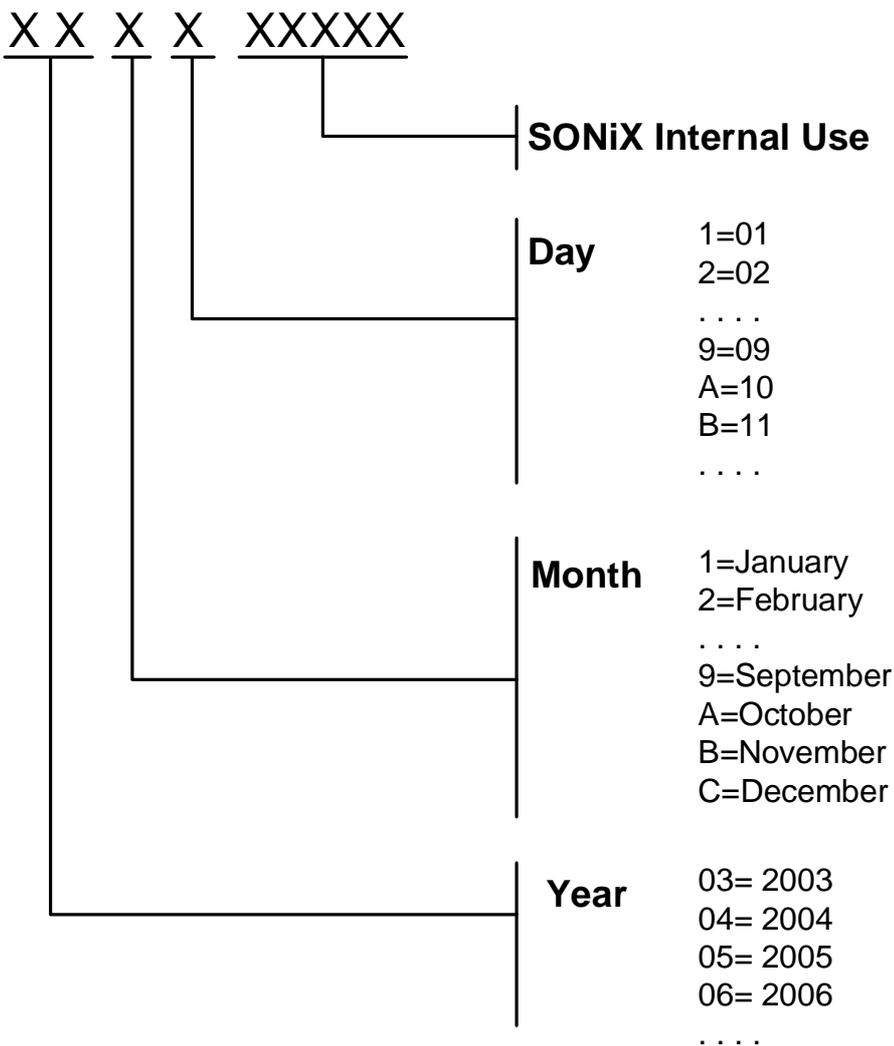
14.2 MARKING INDETIFICATION SYSTEM



14.3 MARKING EXAMPLE

| Name | ROM Type | Device | Package | Temperature | Material |
|-------------|----------|--------|---------|-------------|-----------------|
| SN8P2606PB | OTP | 2608 | P-DIP | 0°C~70°C | PB-Free Package |
| SN8P2606PDB | OTP | 2608 | P-DIP | -40°C~85°C | PB-Free Package |
| SN8P2608XB | OTP | 2608 | SSOP | 0°C~70°C | PB-Free Package |
| SN8P2608XDB | OTP | 2608 | SSOP | -40°C~85°C | PB-Free Package |
| SN8P2608Q | OTP | 2608 | LQFP | 0°C~70°C | PB-Free Package |
| SN8P2608QDB | OTP | 2608 | LQFP | -40°C~85°C | PB-Free Package |

14.4 DATECODE SYSTEM



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