======== CONTENTS ========

AMENDENT HISTORY

Version	Date	Description
Ver 0.1	February 5, 2004	Preliminary spec first issue
Ver 0.2	March 6, 2004	Modify RAM size from 6KW -> 10KW in Page3
Ver 0.3	June 13, 2004	Modify Pin assignment Modify RAM size from 10KW -> 11KW in Page3 Modify int. ROM size from 48KW->64KW in page3 Modify Pin assignments Modify extension bus descriptions, add byte/word mode connection Add new section “Low Voltage Detector” and “Internal Regulator”
Ver 0.4	July 28, 2004	Wording modification of pin assignment in Page 4
Ver 0.5	December 7, 2004	1. Removed UART interface, added USB 1.1 interface 2. Reduce internal RAM size from 11KW to 8KW (4KW for general purpose, 4KW for LCD display buffer) 3. LCD display only support 120x240 / 4 gray-level LCD display. (LCD RAM: 0xB000~0xBFFF) 4. Move general purpose SRAM address to 0xA000~0xAFFF
Ver 0.6	December 10, 2004	1. Page18 Correct word editing error on LCD RAM.
Ver 0.7	December 14, 2004	1. Page21~22 Correct word editing error on LCD RAM.
Ver 0.8	February 25, 2005	1. Correct LCD RAM description on Page 6 2. Modify interrupt sources of “Features” 3. Modify pin assignment 4. Added another 1K word SRAM (0x0000~0x03FF), Page4, 6, 7 5. Added pad information
Ver 1.0	May 30, 2005	1. Modify USB descriptions
Ver 1.1	June 29, 2005	1. Added application circuit 2. Correct some error editing on page9 3. Correct the clock source option table (page8) 4. Remove the RTC 0.125s option (page9) 5. Replace PWM instead of Push-Pull DAC (page11)
Ver 1.2	July 22, 2005	1. Correct bonding pad information (P4.2)
Ver 1.3	July 25, 2005	1. Correct bonding pad information, pin 113 is “CKSEL” and pin111 is “EDWS”

Version	Date	Description
Ver 1.4	April 18 , 2006	1. delete Low clock RC source describe (Page 5,7,8,9) 2. correct support 4-gray LCD (Page 5) 3. add PLL = 1 and CKSEL = 1 is reversed (Page 8) 4. add Note : If chip is halted , SNL320 internal Regulator will be disable (Page 13) 5. correct LCD RAM size 4K and add note: only support 4MHZ LCD clock source (Page 22)

1. INTRODUCTION

The SNL320 is a high performance 16-bit DSP base processor with 16MIPS CPU power. The internal 64K words hi-speed ROM already built-in a hi-performance software voice synthesizer to provides lot of voice effects. Such as hi-decompression engine to support from 1.5kbps ~ 29kbps compression rate for speech and music, multi-channel voice synthesizer to provides 8-channel wave-table melody, or support foreground 1.5kbps~29kbps and background 4-channel wave-table melody.

The standard microprocessor interface allows SNL320 to extend its memory capability, or connect external device. We also built-in a Low Voltage Detector circuit for power management and a USB 1.1 interface for communication with PC.

2. FEATURES

- Power supply:
  2.4V ~ 3.6V (for 2 batteries application)
  3.6V ~ 5.1V (for 3 batteries application)
- Built-in regulator for DSP core
- Built-in 16-bit DSP core
- Software-based voice/melody processing
- Rich Function Instruction Set
- 16 MIPS CPU performances under 16MHz
- Clock system
  - 16MHz crystal or R-C type oscillator for hi-speed system clock
  - 32768HZ crystal oscillator for RTC and low-speed system clock
- Extension bus
  - Standard Byte-mode and Word-Mode bus interface
  - 4 chip select pins for external devices (such as ROM, Flash, SRAM..etc)
  - Maximum 128M-bit addressing capability for signal external memory device
- I/O Ports: 36 I/O pins (P1.0~P1.15, P3.0~P3.15, P4.0~P4.3)
- ROM size: 64K*16 bits
- 9 Interrupt Sources
  - 5 internal interrupt (T0, T1, T2, RTC and USB)
  - 3 external interrupt (P3.0~P3.2)
  - 1 DA/Push-Pull output
- RAM size: 9k*16 bits (including LCD RAM)
  - 5K*16 SRAM size for general purpose
  - 4K*16 for LCD display buffer
- Three 8-bit timers with auto-reload function
- Programmable watchdog timer
- LCD control interface
  - Support 1-bit/4-bit LCD data bus for external LCD driver
  - Share LCD display RAM with internal SRAM, support 240x120 LCD display screen
  - H/W support maximum 4 gray-level LCD display
- Built-in 32768 crystal for Real Time Clock
- Two voice/melody channels or 4 channels wave-table melody
- Built in Push-Pull direct drive circuit and fixed current D/A output
- Sampling Rate: 4KHz ~16KHz
- Built-in software voice synthesizer for multiple bit-rate solution
- USB 1.1 interface provided
- Low Voltage Detector
- Low Voltage Reset

3. PIN ASSIGNMENTS

Symbol	Descriptions	No. of PIn	Pin Count
VDDA	Positive power for OSC	1	1
VSSA	Negative power for OSC	1	2
VDDEBUS	Positive power for EA0~DA22 & ED0~ED15	2	4
VSSEBUS	Negative power for EA0~DA22 & ED0~ED15	3	7
VDDIO2	Positive power for P3.3~P3.15 & P4.0~P4.3	1	8
VSSIO2	Negative power for P3.3~P3.15 & P4.0~P4.3	1	9
PPVDD	Positive power for Push-Pull DAC	1	10
PPVSS	Negative power for P.P. DAC	2	12
VDDIO1	Positive power for P1.0~P1.15 & P3.0~P3.2	1	13
VSSIO1	Negative power for P1.0~P1.15 & P3.0~P3.2	1	14
CVDD	Positive power for DSP core logic	2	16
CVSS	Negative power for DSP core logic	1	17
RVDD	Positive power for regulator	1	18
VOUT	Regulator voltage output	1	19
PLLCAP	Cap pin for PLL	1	20
XIN	High speed clock crystal input / RC-type oscillator input	1	21
XOUT	High speed clock crystal output / RC-type oscillator input	1	22
LXIN	Low speed clock crystal input	1	23
LXOUT	Low speed clock crystal output	1	24
CKSEL	Crystal/RC-type oscillator select for high speed clock	1	25
PLLEN	PLL Enable/Disable control	1	26
BP0	Push-Pull DA output	1	27
BN0	Push-Pull DA output	1	28
VO0	DAC output	1	29
RSTB	Chip reset	1	30
TEST	For test only	1	31
EA0~EA22	Address bus of extension bus	23	54
ED0~D15	Data bus of extension bus	16	70
WR\	Write signal of extension bus	1	71
RD\	Read signal of extension bus	1	72
EDWS	Extension bus width select 0: 8-bit (byte mode) 1: 16-bit (word mode)	1	73
D+	USB Data +	1	74
D-	USB Data -	1	75
PWR+	USB power +	1	76
PWR-	USB power -	1	77
P1.0~P1.15	General I/O port P1.0~P1.15	16	93

Symbol	Descriptions	No. of PIn	Pin Count
P3.0~P3.15	General I/O port P3.0~P3.15 P3.0: INT0 P3.1: INT1 P3.2: INT2 / IR output P3.3: NCSB P3.4: CLE P3.5: ALE P3.6: R/B\ P3.7: WPB P3.8: CS3/EA23 P3.9: CS2 P3.10: CS1 P3.11: CS0 P3.12: LACD P3.13: LCLK P3.14: LP P3.15: FP	16	109
P4.0~P4.3	General I/O port P4.0~P4.3 LCD data bus	4	113

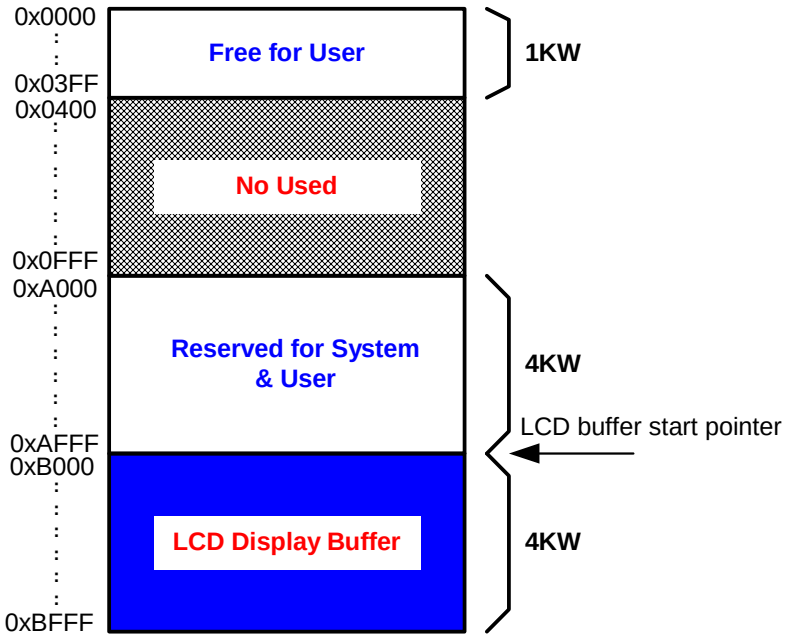
4. MEMORY

4.1 Internal ROM

SNL320 provides hi-compression algorithm to compress voice data in order to save more memory size. So all the de-compression program are built in the internal ROM of SNL320 and system will reserved some necessary ROM space for those de-compression program automatically once user active the de-compression function. There are totally 64K words of SNL320 internal ROM, user can built-in his own program in the internal ROM for his application except necessary space for de-compression program.

4.2 Internal RAM

The internal totally 9K words RAM will be separated into two parts, the SRAM regions 0xA000~0xAFFF and 0x0000~0x03FF are reserved for system and user's application, the SRAM regions 0xB000~0xBFFF is reserved for LCD display buffer. User has to define the actual LCD display buffer region by set LBUFL (LCD display buffer register).



5. Clock System

SNL320 is a dual clock system that it both provides high-speed clock (16MHZ) and low-speed clock (32768HZ). There two different way to get the hi-speed clock, one is generate by external 16MHZ crystal and another way is through external 6MHZ pumping to 16MHZ by the internal PLL circuit.

The pin option “PLLEn” is used to enable/disable internal PLL circuit.

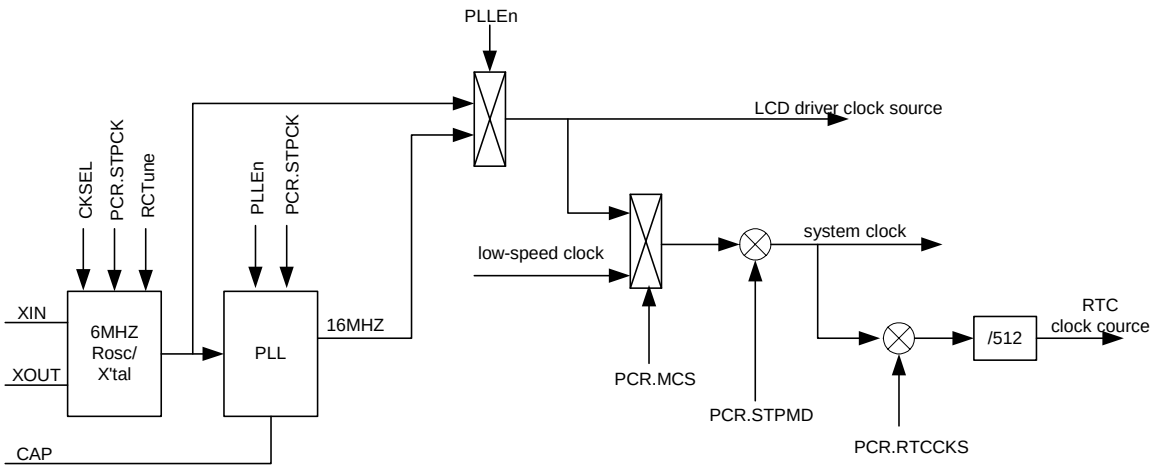


Figure-1 Clock system block diagram

5.1 Normal Mode

The normal mode means CPU main clock source is comes from 16MHZ Rosc or crystal hi-speed clock source, so SNL320 is run in full speed. There are two pins option "CKSEL" and "PLLEn" to select Rosc/crystal and enable/disable PLL circuit.
The detail setting of hi-speed clock is shown as following table.

CKSEL	PLLEn	Descriptions
0	0	16MHZ X'tal for hi-speed clock source
0	1	6MHZ X'tal and pumping to 16MHZ for hi-speed clock source. (for USB application)
1	0	16MHZ Rosc for hi-speed clock source
1	1	reserved

5.2 Low-speed mode

This is a special operation mode of SNL320, the hi-speed clock is disable and main clock of SNL320 is comes from low-speed clock source (32768HZ). It will save more power consumption when chip works on this low-speed mode and this low-speed clock can select 32768HZ crystal for clock source.
In additional, this low-speed clock also used to calibrate the hi-speed clock once the high-speed clock source is comes from Rosc.

5.3 Stop Mode

In stop mode, all the system clocks are stop (16MZH & 32768HZ) and chip entry a very low power consumption state. Chip will wake-up from stop mode once any IO state change or external interrupt occurs.

5.4 Suspend Mode

In suspend mode, the hi-speed clock still working but chip is hold until any IO toggle or external interrupt occurs. That means, the power consumption only come from HXOSC circuit and LCD driver interface refresh circuit.

5.5 Watch Mode

This mode is for some real time clock application, users have to add a 32768HZ crystal to realize RTC function. Considering to saving power consumption, user should stop the hi-speed clock source (16MHZ) and enable the low-speed clock source. Then chip will entry power down mode but the low-speed clock still working and wake-up chip once the RTC period is happened in order to fresh the RTC timer.

There are four options for RTC interrupt period, users can select 0.25sec/0.5sec and 1sec through the RTC control register.

If chip is in power-down mode and interrupt enable is active for RTC, then chip will be wake-up from power-down mode per 0.25/0.5/1 second.

6. POWER ON RESET

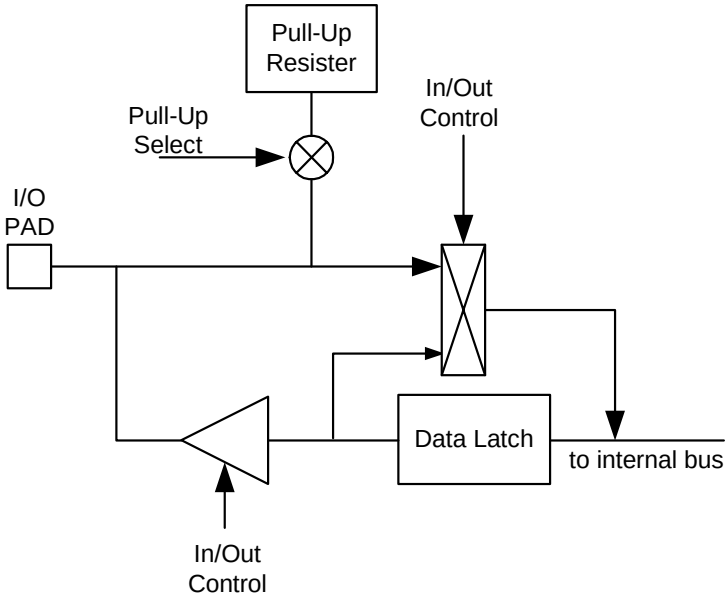
When “L” level appears on RESET PIN, the chip will enter RESET state.
After reset, the chip does not execute the first instruction until counting 2^{17} clock cycles. It takes around 8.2ms at 16MHz. (crystal for clock source), and the location of the first instruction after RESET is 0x000000. In additional, all the contents of SRAM will be unchanged during RESET stage.

7. I/O PORT

SNL320 provides totally 36 I/O pins (P1.0~P1.15, P3.0~P3.15, P4.0~P4.3). The input pull-high resistor of each pin can be programmed by port pull-high register and the direction of I/O port is selected by port direction register. The I/O port P1.0~P1.15 can wake the chip up from the stop mode and watch mode.

These 36 programmable I/O pins provides not only a simply input/output function but also can configure to be chip select pins of extension bus, LCD driver interface and NAND flash interface. For the detail please refer to following sections.

The internal structure of I/O pins is showed in **Figure-2**.



I/O Configuration of Port1, Port3 and Port4

Figure-2

In some applications (e.g., Infra Red, IR), an output port needs to be modulated a carry signal. In the cases, the routine of modulation will occupy too many CPU computations. Thus, a modulation circuit is built in chip to reduce CPU's loading.

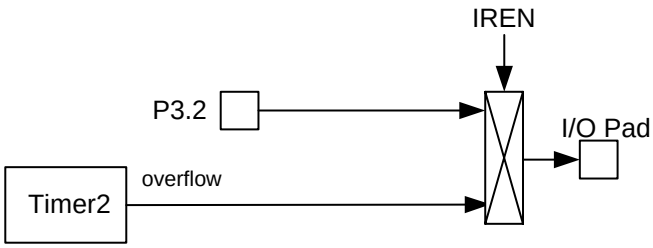


Figure-3

The modulation function will be active when the control bit "IREN" set to "1". And setting timer2 can generate the frequency of carry signal.

8. TIMER/COUNTER

SNL320 provides three 8-bit timer/event counters (T0/T1/T2). Each timer is 8-bit binary up-count timer with pre-scalar and auto-reload function. Timer 0 (T0) was used when voice playing, so user should avoid to use T0.

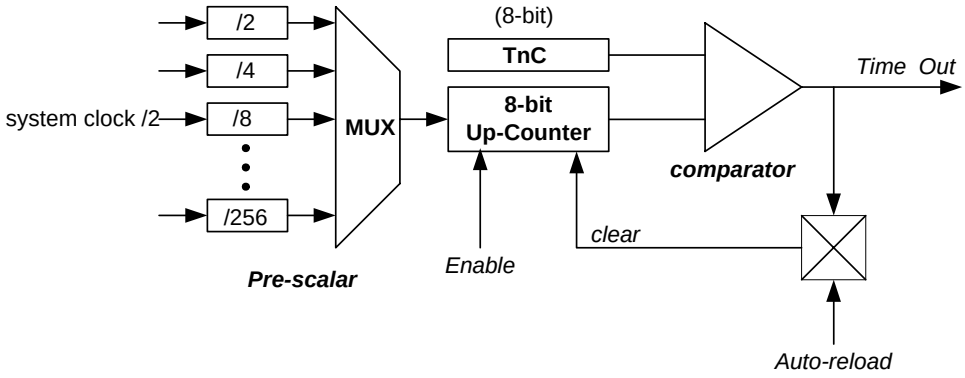


Figure-4

9. DA & Push-Pull

To play out voices, SNL320 contains two different solutions for the user's applications, DAC and Push-Pull. The user can choose one of these two solutions in this design. Only one function can be activated at one time.

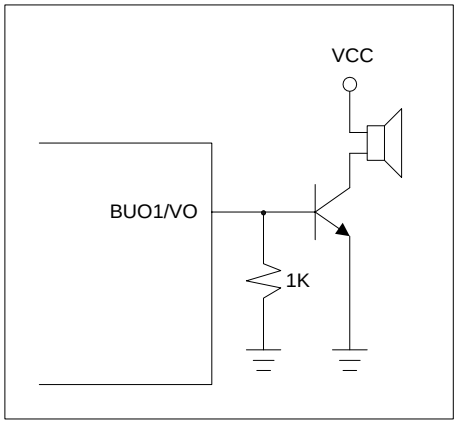
9.1 DAC

A 10-bit current type digital-to-analog converter is built-in SNL320. The relationship between input digital data and output analog current signal is listed in the following table. Also, the recommended application circuit is illustrated as follows.

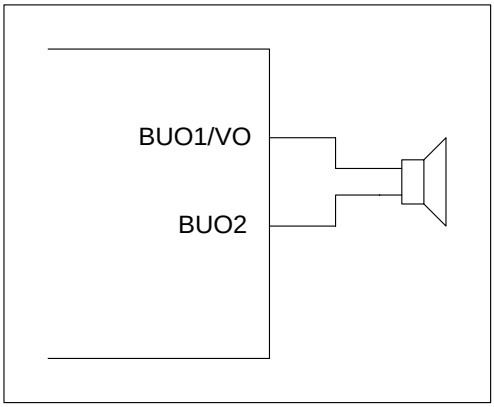
Input data	Typical value of output current (mA)
0	0
1	3/1024
…	
n	n*(3/1024)
…	
1024	3

9.2 Push-Pull

A Push-Pull Direct Drive circuit is built-in SNL330. The maximum resolution of Push-Pull is 10 bits. Two huge output stage circuits are designed in SNL330. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.



DAC output

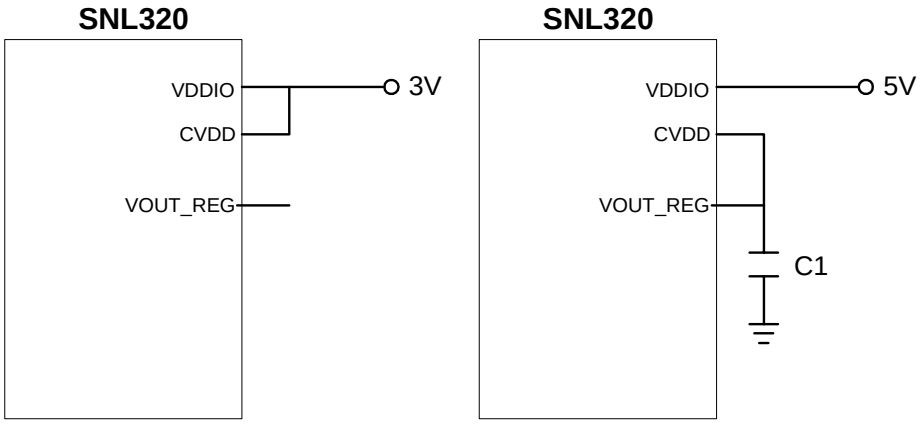


Push-Pull output

10. Internal Regulator

The power system of SNL320 can be separated into two groups, one is 3V and another one is 5V. The power of core logic and SRAM, ROM is comes from 3V power group. And the power of all I/O, DA/Push-Pull, clock system is comes from 5V power group.

Considering user's application, SNL320 built-in a regulator to solve the different power problem. Please refer to the following connection diagram.



3V power system **5V power system**

For 3V power system (2 batteries application), all the power pins should be connected together.

For 5V power system (3 batteries application), the power pin of core logic CVDD pin should be connected to VOUR_REG in order to get an accurate 2.8V power.
Once chip entry power down mode, the regulator will also turn off automatically. And this regulator also built-in a LVD circuit to detect the power dropping of VOUT_REG. The regulator will auto turn on to re-charge the power of external CAP C1 when the voltage of VOUT_REG is lower then 2.2V, it will make sure to provides enough power for CVDD to keep the value of SRAM.
Note : If chip is halted , SNL320 internal Regulator will be disable

11. Low Voltage Detector

SNL320 built in a low voltage detector for power management. It provides four different detect level, 2.3V, 2.5V, 2.8V and 3.1V. User can set an expect detect level through the PCR control register and polling the acknowledge bit to get the current power level is higher or lower then the detect level. Each detect level is designed by schmitt trigger architecture, that's means each detect level has a detect window.
For example, the detect window of detect level 2.3V is 2.24V ~ 2.36V. When the VDD power down below 2.24V, the detect bit of PCR register will be set to 1. Once VDD power is recovered and must be higher then 2.36V, then detect bit is clear by system.

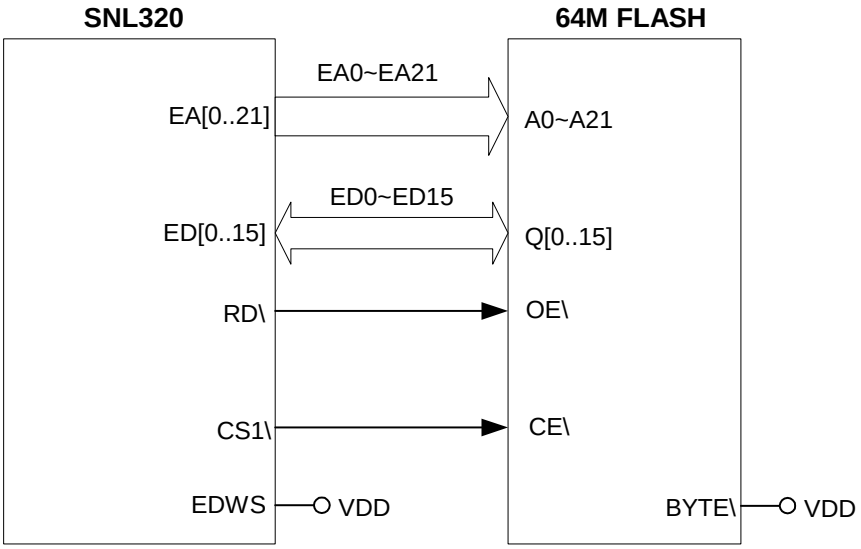
Detect level	Voltage window of schmitt trigger
2.3V	2.24V ~ 2.36V
2.5V	2.44V ~ 2.57V
2.8V	2.72V ~ 2.88V
3.1V	3.01V ~ 3.19V

12. EXTENSION BUS

SNL320 built-in a standard micro-controller interface extends the memory capability through the extension bus. In additional, SNL320 both provides byte mode and word mode access bus for external memory device in order to improve the efficiency.
This extension bus also allows users to connect different external devices for his own application, such as ROM, RAM, NAND flash, 8-bit interface LCD controller etc.
There are 4 chip select pins for external devices, so totally SNL320 can connect 4 different devices. The maximum addressing capability of each external device is 64M-bit except CS0. Because the ROM bank of CS0 is shared with internal ROM of SNL320, so the maximum addressing capability of CS0 is only 32M-bit. In additional, user can put his program into each external memory device not only data.

12.1 Word Mode Connection

Most of hi-density memory both provides word mode access, so SNL320 also support word mode access bus by the pin option “EDSW”. Once the pin “EDSW” is connected to VDD, means the bus width of extension bus will turn to be 16-bit width, the connection diagram is shown as bellow. In word mode bus access, SNL320 can fetch a complete OP code or data through the 16-bit width bus at one time, and it is helpful to improved the CPU efficiency when CPU running the program from external memory device. Most important, once the word access is selected, all the data access will fixed at 16-bit mode. So if user connected a 8-bit width external device, the bus pin ED[8..15] of extension bus don’t need to be connected.



Flash Memory Word Mode Connection

Note: The bit14 of EBCR control register MUST set to be “1”.

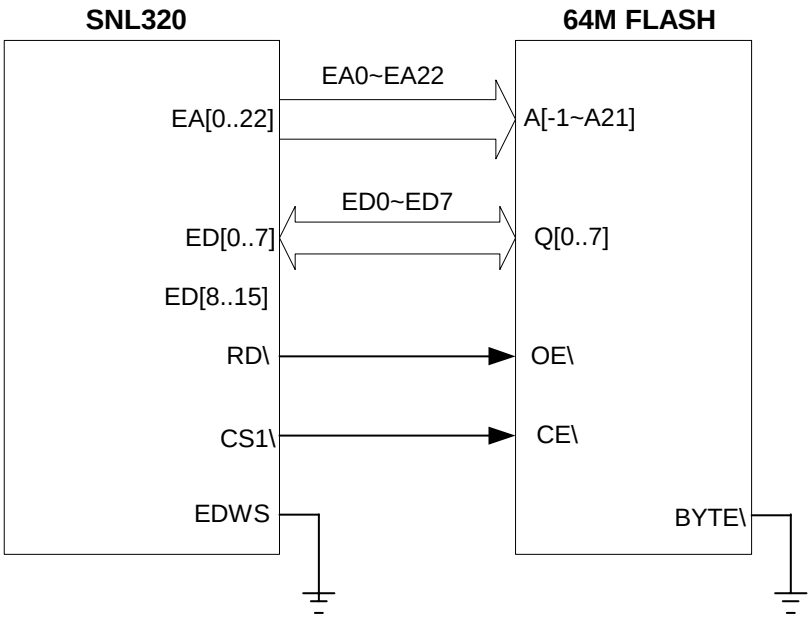
12.2 Byte Mode Connection

Considering the bus interface of some external devices and memory are also only 8-bit bus width, so SNL320 also support the byte mode access bus for this kind of device. In byte mode, only data pins ED[0..7] are valid and ED[8..15] are no used.

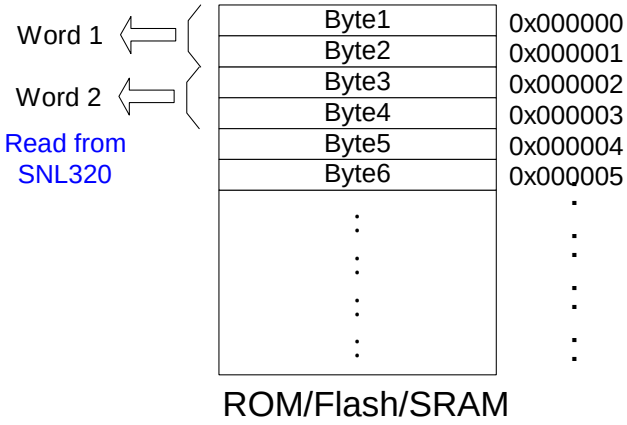
In byte mode connection, SNL320 provides two different modes for data access, one is 8-bit mode and another is 16-bit mode. The detail description is shown as following section.

12.2.1 16-bit Mode

In 16-bit mode, all the data and OP code fetch are base on 16-bit data width. In another hand, SNL320 will fetch data or OP code from external memory two times automatically, in order to get a complete 16-bit width data.



DSP 16-bit mode (for flash Byte mode connection)

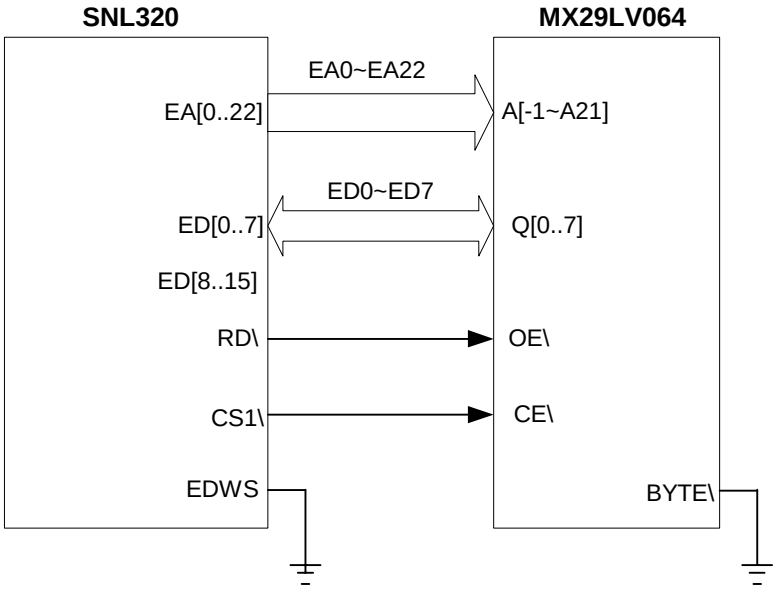


Note: The bit14 of EBCR control register MUST set to be "1".

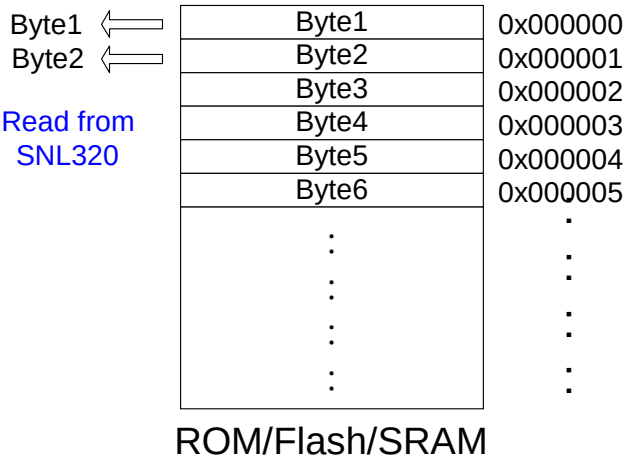
12.2.2 8-bit Mode

SNL320 also reserved a 8-bit mode data access for user's application. The only one different is the addressing capability of 8-bit and 16-bit mode. In 16-bit mode, the maximum addressing capability of each chip select pin (CS1~CS3) is 64M-bit (CS0 is only 32M-bit) because the address pin EA[22].

In 8-bit mode, the EA[22] is a invalid address pin, so all the addressing capability calculation is only a half of 16-bit mode.



DSP 8-bit mode (for flash Byte mode connection)



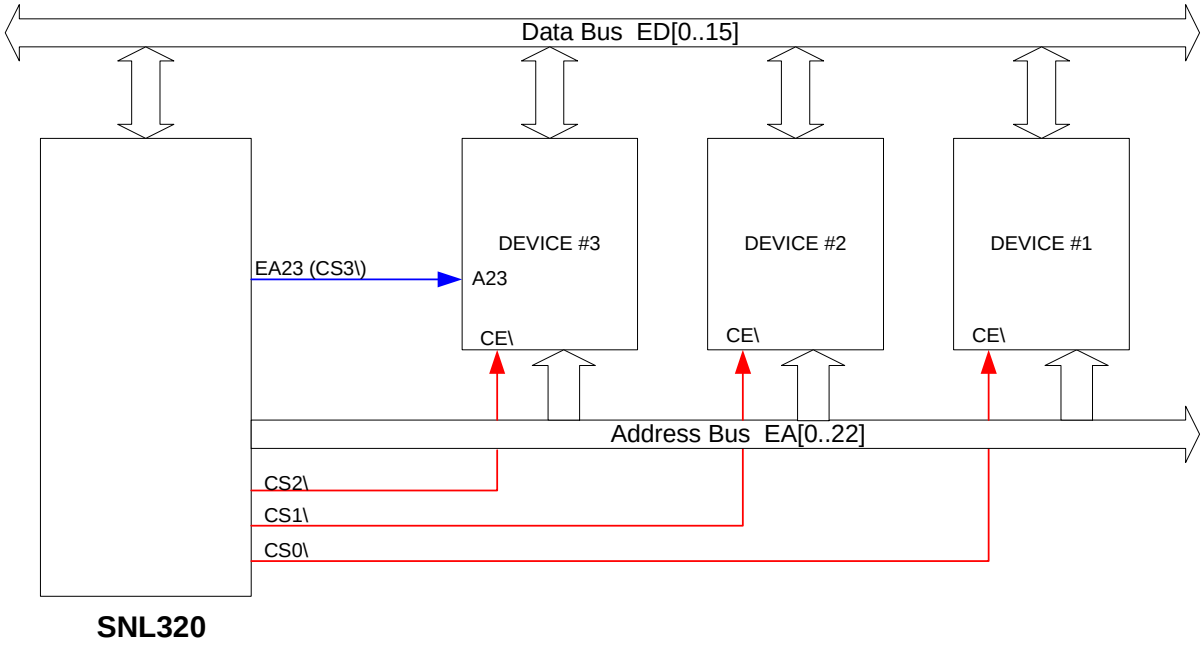
Note: The bit14 of EBCR control register MUST set to be "0".

Device No.	Start address	End Address	Memory Size
Internal ROM	0x0000000	0x000FFFF	64K words
Reserved	0x0010000	0x01FFFFF	1984K words
1st external device	0x0200000	0x03FFFFF	2M words
2nd external device	0x0400000	0x07FFFFF	4M words
3rd external device	0x0800000	0x0BFFFFF	4M words
4th external device	0x0C00000	0x0FFFFFF	4M words

Table-1 Addressing Capability (16-Bit Mode)

12.3 Maximum Memory Expend

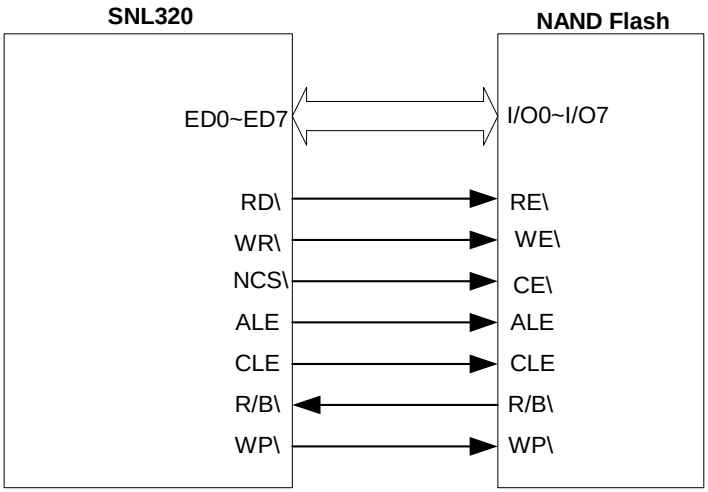
SNL320 also provides a special function extend the memory size from 64M-bit up to 128M-bit for single external device. The chip select pin “CS3” can be turn to the address pin “A23” once user enable the control bit of “CS3” & “EA23” of extension bus control register.



12.4 NAND Flash Interface

SNL320 provides a special function to access data from the external NAND flash memory. The following table is shown the relative pins of NAND flash memory interface. P3.3~P3.7 will becomes to be the control signal of NAND flash memory once the property control register was setting, and data bus of NAND flash memory are shared with the data bus D0~D7 of extension bus. All the data read/write are easy to implement by the software.

I/O Pin	Pin Name	Direction	Descriptions
P3.3	NCSB	O	NAND flash memory chip enable pin
P3.4	CLE	O	Command latch enable
P3.5	ALE	O	Address latch enable
P3.6	R/B\	I	NAND Flash memory Ready / Busy output
P3.7	WPB	O	Write protect
RD\	RD\	O	Read signal
WR\	WR\	O	Write signal
ED0~ED7	D0~D7	IO	Data bus D0~D7



13. USB INTERFACE

The SNL320 provides a USB 1.1 interface, user can download/upload data from/to PC through this USB interface. It is support control transfer and bulk transfer.
SNL320 provides twin buffers for data or command transition and the buffer size of those twin buffers is 64bytes.

14. LCD INTERFACE

14.1 LCD Controller Interface (8-bit interface)

The extension bus of SNL320 supports not only external memory device but also 8-bit 8080/6800 microprocessor interface for external LCD controller which already built-in LCD display RAM. User should enable extension bus before driving external LCD driver, and define the chip select pin you used to connect to LCD driver in EBC register.
In 8-bit interface LCD controller, LCD display data is stored in LCD controller. Any change of LCD display is sent out to external LCD driver's RAM by addressing different SRAM space. The interface emulates the 8080/6800-series interface to speed up the interface data moving processing.
Figure-5 and **Figure-6** are the timing diagrams between SNL320 and LCD controller by using 8-bit 8080/6800 interface.

8080-series Interface:

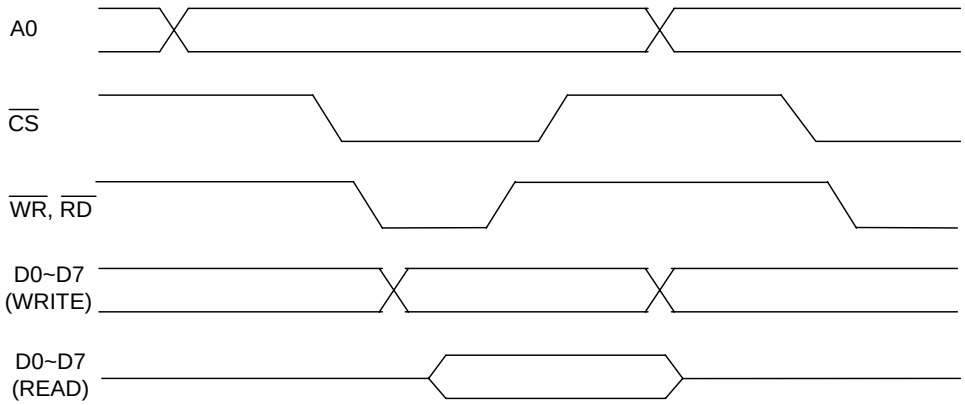


Figure-5

6800-series Interface:

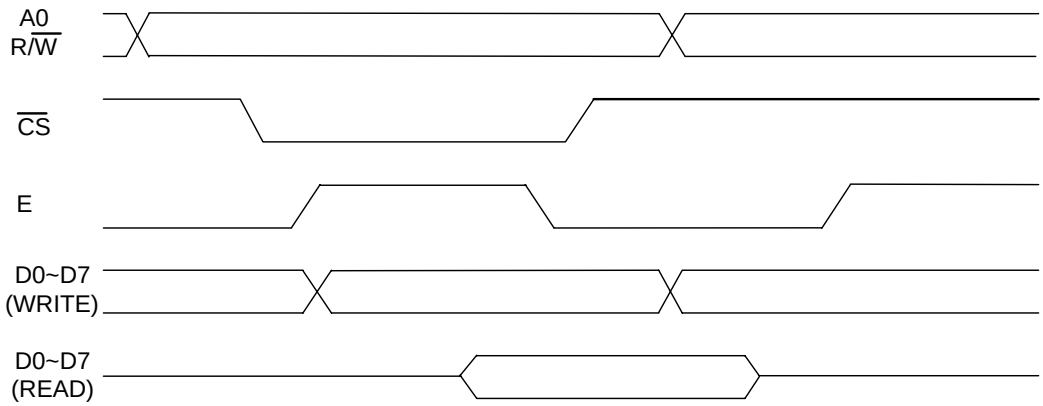
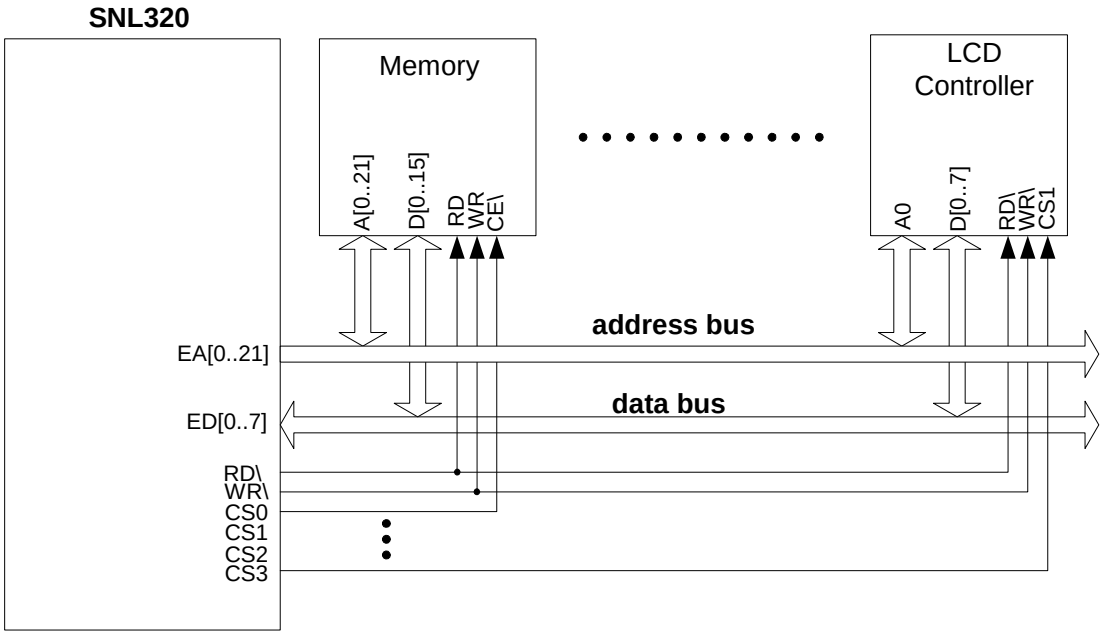
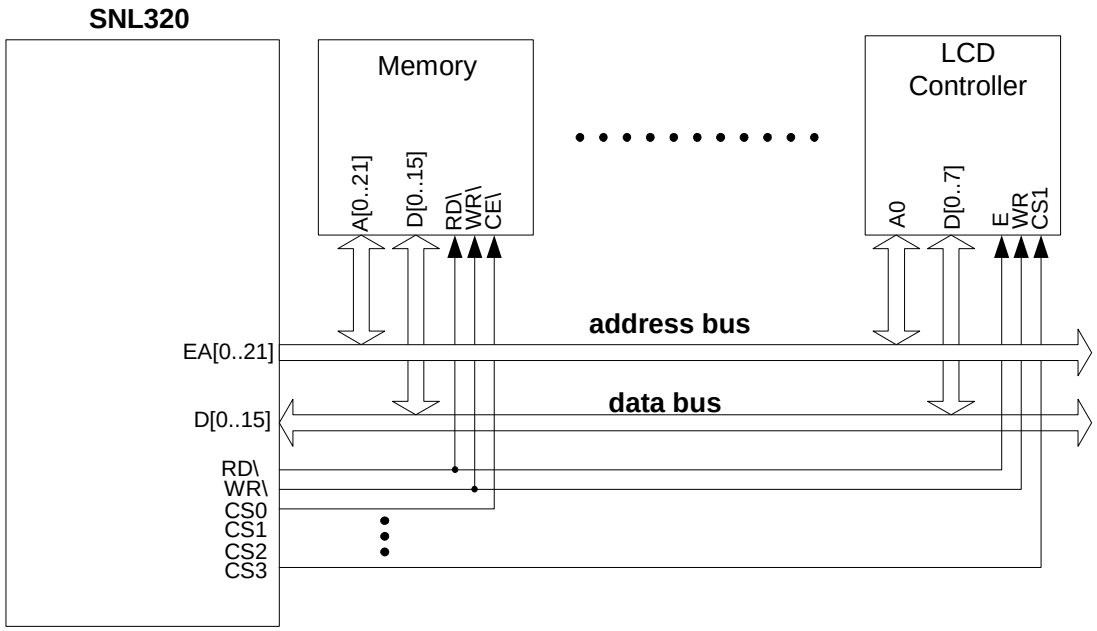


Figure-6

Figure-7 and **Figure-8** show out the system connection of 8080/6800 LCD interfaces between SNL320 and LCD controller.



8080 LCD controller interface
Figure-7



6800 LCD controller interface
Figure-8

14.2 LCD Driver Interface (1/4 bits interface)

SNL320 supports not just 8-bit interface but also 1-bit/4-bit interface for LCD driver. For this kind LCD driver doesn't include display RAM. All the display data is stored in host CPU. So SNL320 has to specify a dedicate interface to drive LCD driver. Besides, SNL320 reserves 4K words LCD Buffer (0xB000~0xBFFF) for LCD display. Hardware circuit will send accurate signal to LCD driver automatically once the 1-bit/4-bit LCD driver interface is enabled. The internal 4K words SRAM can support maximum 240x120 dots LCD display with 4-grey level effect.

Note : only support 4MHZ LCD clock source

14.3 Control Signals

P3.12~P3.15 & P4.0~P4.3 can be configured to be 1-bit/4-bit interface for LCD driver just by property setting control register. **Table-2** shows the relation between P3.12~P3.15, P4.0~P4.3 and LCD driver interface.

I/O Pin	Pin Name	Descriptions
P3.12	LACD	LCD alternating signal
P3.13	LCLK	Dot clock
P3.14	LP	Line signal
P3.15	FP	First line marker
P4.0	LD0	LCD data output D0
P4.1	LD1	LCD data output D1
P4.2	LD2	LCD data output D2
P4.3	LD3	LCD data output D3

Table-2

14.4 LCD RAM Mapping

The RAM region from 0xB000 to 0xBFFF totally 4K*16 is reserved for LCD display buffer, user just need to copy the LCD display pattern data into this area then chip will display the pattern on LCD panel automatically.

There is a special register LBUF to specify the LCD display buffer start address.

Calculating formula of start address

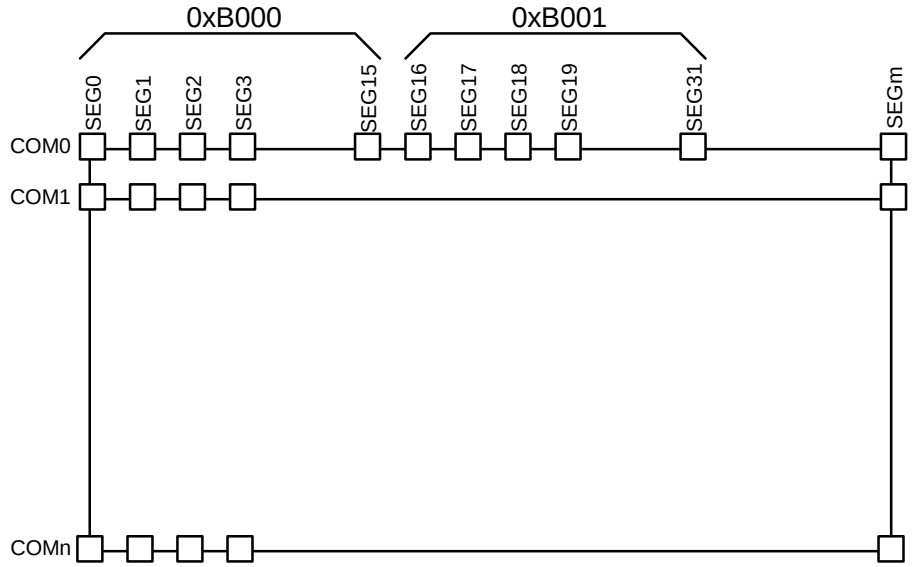
49152-(SEG numbe/16)*COM number => for B/W

49152-(SEG numbe/16)*COM number*2 => for 4 gray levels

NOTE:

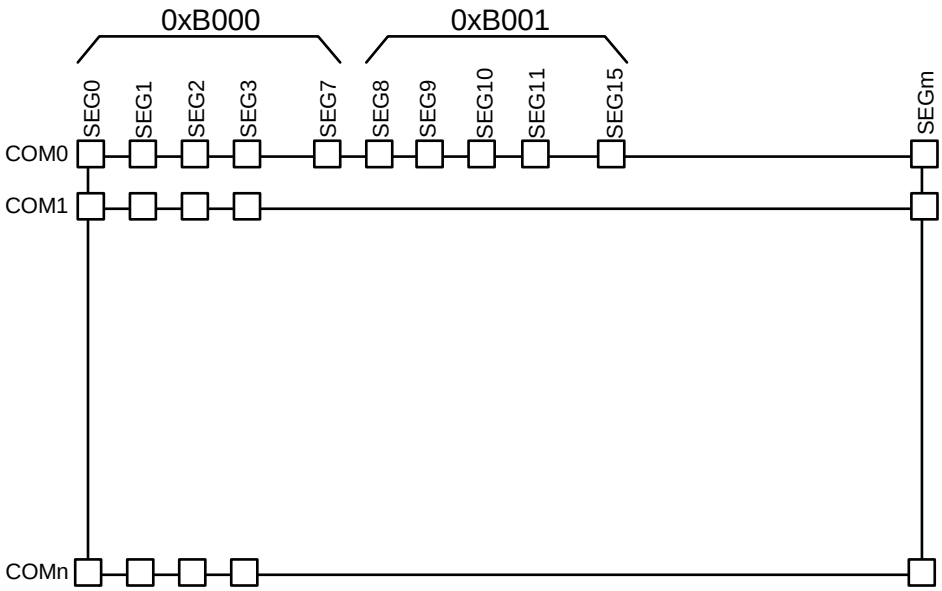
SEG number must be the multiple by 8.

For B/W LCD display, each bit of display memory mapping to a pixel in the LCD panel. Please refer to following diagram, the display data of SEG0 ~ SEG15 at COM0 is mapping to bit0~bit15 of display memory 0xB000



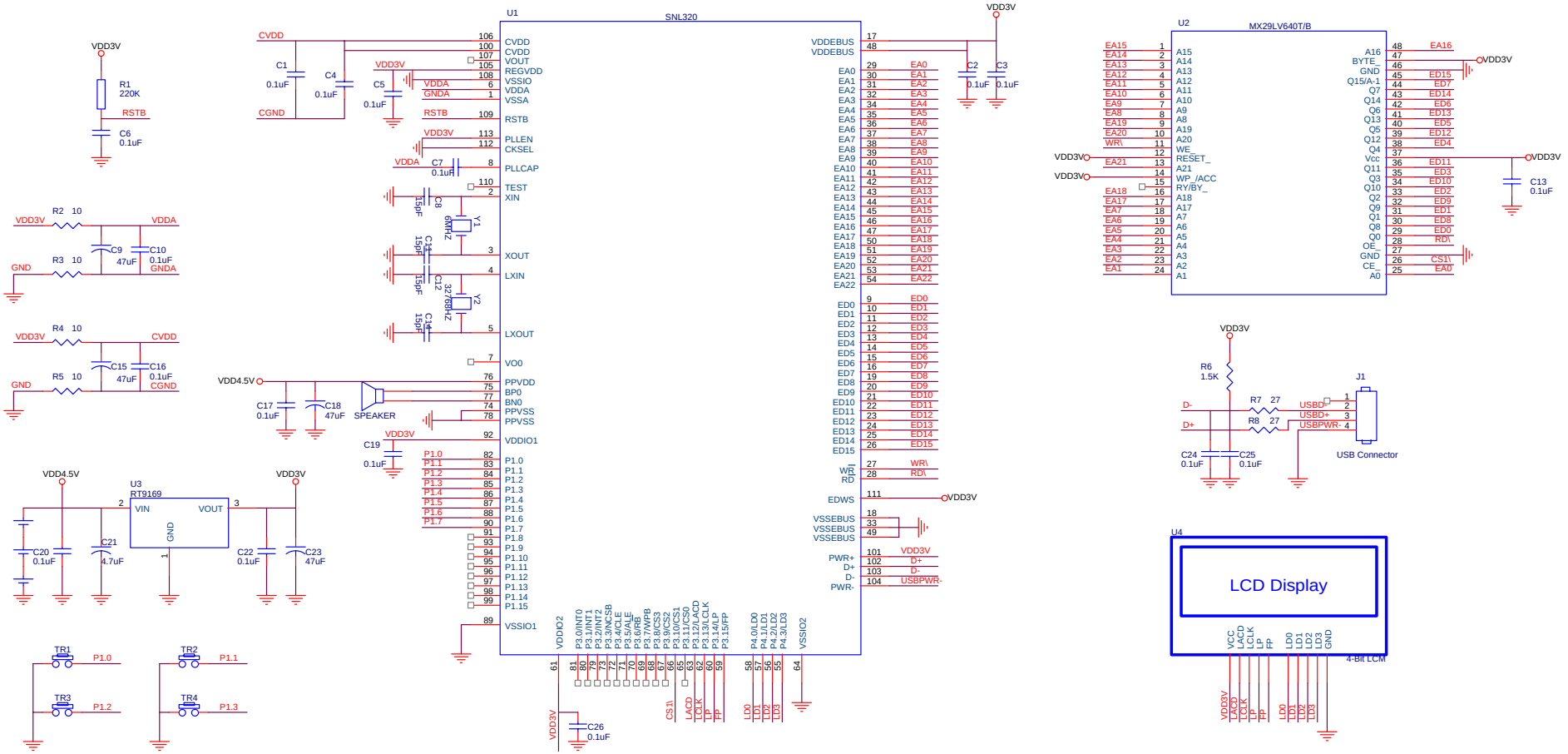
LCD screen format (B/W)

For 4-gray level LCD display, each display pixel takes two bits space to store the gray level display data. Please refer to following diagram, the display data of SEG0 ~ SEG7 at COM0 is mapping to bit0~bit15 of display memory 0xB000.



LCD screen format (4-gray level)

15. Application Circuit



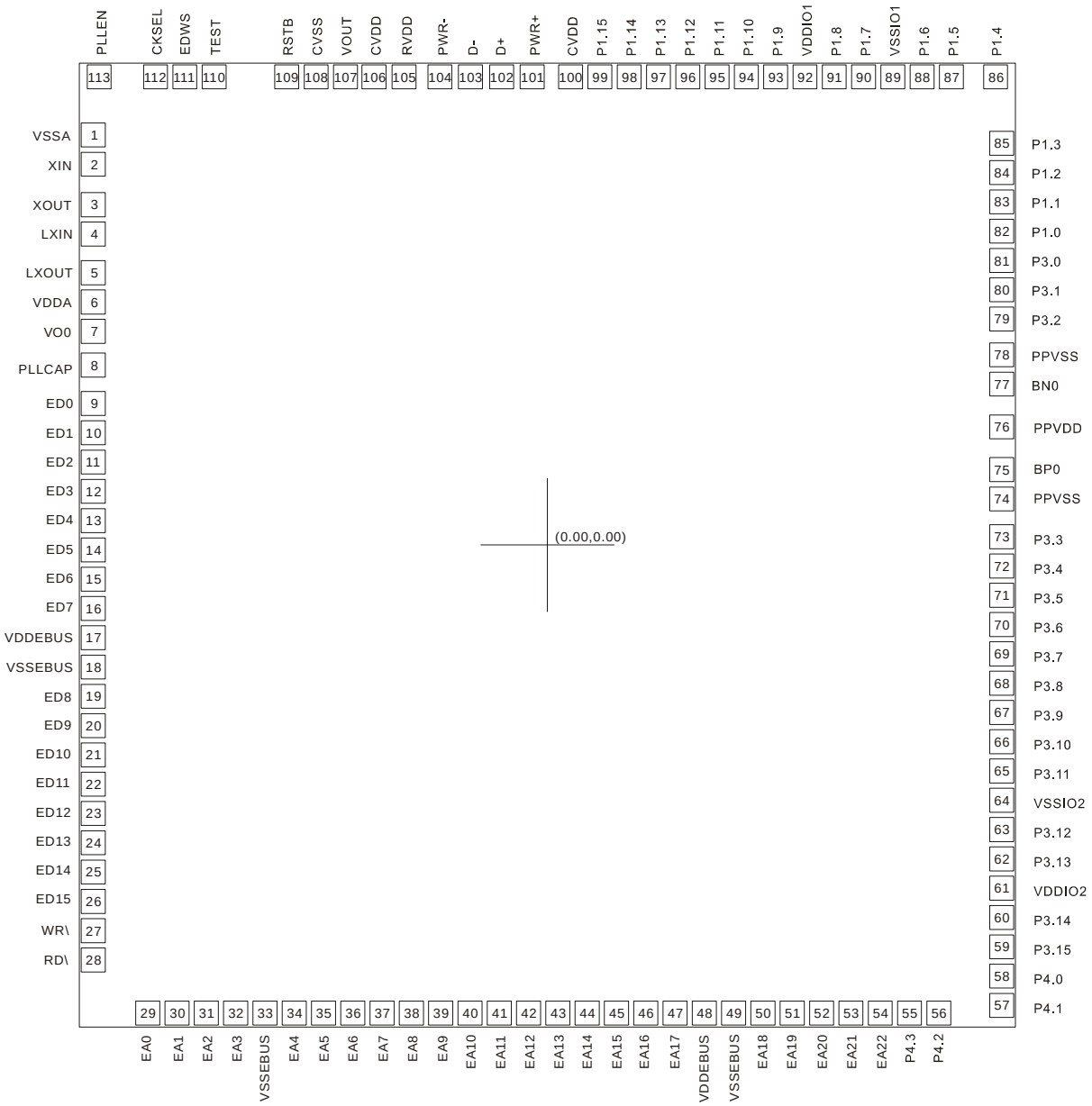
16. ABSOLUTE MAXIMUM RATINGS

Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	6.0	V
Input Voltage	V_{IN}	GND-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55	^{o}C
Storage Temperature	T_{STG}	-55.0	125.0	^{o}C

17. ELECTRICAL CHARACTERISTICS

Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	-	3.6	V	
	V_{DD}	3.6	-	5.1	V	
Standby current	I_{SBY}	-	2.0	-	*u*A	V_{DD}=3V, no load
Operating Current	I_{OPR}	-	10	-	mA	V_{DD}=3V, no load
Pull-Up resistor of P1, P3, P4	R_{PU}	-	800	-	KΩ	V_{DD}=3V, no load
Input current of P1, P3, P4	I_{IH}	-	-	10.0	*u*A	V_{DD}=3V,V_{IN}=3V
Drive current of P1, P3, P4	I_{OD}	-	**6**	-	*m*A	V_{DD}=3V,V_{O}=2.4V
Sink Current of P1, P3, P4	I_{OS}	-	**8**	-	*m*A	V_{DD}=3V,V_{O}=0.4V
Drive current of Buo1	I_{OD}			-	*m*A	V_{DD}=3V,Buo1=1.5V
Sink Current of Buo1	I_{OS}			-	mA	V_{DD}=3V,Buo1=1.5V
Drive Current of Buo2	I_{OD}			-	mA	V_{DD}=3V,Buo2=1.5V
Sink Current of Buo2	I_{OS}			-	mA	V_{DD}=3V,Buo2=1.5V
Oscillation Freq. (crystal)	F_{OSC}	-	16.0	-	MHz	V_{DD}=3V

18. Bonding Pad



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