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History

Version	Release Date	Descript
1.0	8/29/2006	1. First release.
1.1	8/31/2006	1. Add contents page.
1.2	9/6/2006	1. Add electrical characteristics descript.
1.3	9/7/2006	1. Modify feature descript error. 2. Redefine pin name. 3. Modify system clock descript. 4. Modify electrical characteristics. 5. Add history page. 6. Add Bonding PAD map.
1.4	1/16/2007	1. Add Application circuit.
1.5	01/25/2007	1. Remove current DAC function.
1.6	02/26/2007	1. Remove current DAC output pin.
1.7	03/01/2007	1. Add ROSC application circuit.
1.8	03/06/2007	1. Modify application error. 2. Add Regulator section.
1.9	04/25/2007	1. Modify Regulator feature 2. Add \RC after Pin Assignment : Lxin 3. Add ROSC Input description 4. Modify Slow mode current
2.0	05/08/2007	1. Add low clock ROSC application circuit.
2.1	05/26/2007	1. Modify low clock ROSC resister value.
2.2	08/28/2007	1. Modify Reset register value.
2.3	05/06/2008	1. Modify power input of AP circuit.
2.4	07/25/2008	1. Modify Application circuit. Connect VSSIO2 to GND.
2.5	08/04/2008	1. Modify Application circuit. Switch capacitance 0.1uF and 47uF location of VDDA, VDDIO0, VDDPP and VDDIO1.
2.6	09/01/2008	1. Added description about power range.
2.7	07/20/2009	1. Add schematic and notice about application uses crystal without 32768 crystal. 2. Modify power supply at feature section. 3. Add “bonding info” for substrate.

1. INTRODUCTION

The SNC749 is a simply chip base on new DSP technology. SNC749 provide simply and easy control functions for system manufactory. SNC749 also is a high performance voice IC. That is built-in 64K word high speed ROM, and by different model to built-in 64K word, 448K words low speed ROM, the maximum program size is full ROM size include high-speed and low-speed ROM.

The SNC749 have three timer, one real time clock and one watchdog timer and built-in a hi-performance software synthesizer to provide lot of voice effects, such as hi-decompression engine to support from 1.5Kbps ~ 32Kbps compression rate for speech and music, multi-channel voice synthesizer to provide 12-channel wave table melody.

2. FEATURES

- Power supply:
  2.4V ~ 3.6V (for 2 batteries application)
  2.7V ~ 5.1V (for 3 batteries application)
- Built-in a new 16-bit DSP core with 16 MIPS CPU performance
- Software-based voice/melody processing
- Rich Function Instruction Set
- System Clock
  - 16MHz crystal or R-C type oscillator for system clock
- I/O Ports:
  - 24 I/O pins (P0.0~P0.15, P1.0~P1.7)
  - P0.15 with IR carrier signal
- RAM size: 4K*16 bits
- ROM size: 512KW
  - High performance program ROM: 64K*16 bits
  - Low speed ROM: 448KW
- Maximum program size: Full ROM Size
- 3 Timer, 1 RTC, 1 WDT
  - Timer With Individual pre-scalar and auto-reload function
  - RTC with 0.25/0.5/1 sec period
  - Watchdog Timer
- 9 Interrupt Sources
  - 4 for Internal Timer (timer0, 1, 2 and RTC)
  - 4 for External (P0.0~P0.3)
  - 1 for DA (Push Pull DAC)
- Two voice channels / 12 melody channels
- Three 8-bit timer with auto-reload function
- Built in a 10-bit Push-Pull DAC direct drive circuit
- Internal regulator provided

- Low Voltage Reset
- Low Voltage Detect
- Sampling Rate: 8KHz ~16KHz
- Built-in software voice synthesizer (LRC5：1.5K, 1.72K, 2K, 2.4K, 3K, 4K　DRC：5K, 6K SN：8K　MSADPCM：35K　PCM：80K　AUDIO32_16K：16K, 20K, 24K, 28K, 32K)
- Built-in software melody synthesizer includes the dual-tone melody and 12-channel wave-table melody.

3. PIN ASSIGNMENT

Pin No.	Symbol	I/O	Descriptions
1	Test	I	Test Pin for testing using
2	VSSIO2	I	Negative power supply
3	CVSS	I	Negative power supply for core circuit
4	RST	I	Chip reset
5	CKSEL	I	Crystal/RC-type oscillator select for high speed clock
6	VDDIO2	I	Positive power supply
7	CVDD	I	Positive power supply for core circuit
8	REGOUT	O	Regulator voltage output
9	VSSA	I	Negative power supply
10	XIN	I	High speed clock crystal input
11	XOUT	O	High speed clock crystal output
12	LXIN	I	Low speed clock crystal input \ RC
13	LXOUT	O	Low speed clock crystal output
14	VDDA	I	Positive power supply
15	NC	-	-
16	P0.0	I/O	I/O Port 0
17	P0.1	I/O	I/O Port 0
18	P0.2	I/O	I/O Port 0
19	P0.3	I/O	I/O Port 0
20	VSSIO0	I	Negative power supply
21	P0.4	I/O	I/O Port 0
22	P0.5	I/O	I/O Port 0
23	P0.6	I/O	I/O Port 0
24	P0.7	I/O	I/O Port 0
25	VDDIO0	I	Positive power supply
26	P0.8	I/O	I/O Port 0
27	P0.9	I/O	I/O Port 0
28	P0.10	I/O	I/O Port 0
29	P0.11	I/O	I/O Port 0
30	VSSIO0	I	Negative power supply

Pin No.	Symbol	I/O	Descriptions
31	P0.12	I/O	I/O Port 0
32	P0.13	I/O	I/O Port 0
33	P0.14	I/O	I/O Port 0
34	P0.15	I/O	I/O Port 0
35	P1.0	I/O	I/O Port 1
36	P1.1	I/O	I/O Port 1
37	P1.2	I/O	I/O Port 1
38	P1.3	I/O	I/O Port 1
39	VDDIO1	I	Positive power supply
40	P1.4	I/O	I/O Port 1
41	P1.5	I/O	I/O Port 1
42	P1.6	I/O	I/O Port 1
43	P1.7	I/O	I/O Port 1
44	VSSIO1	I	Negative power supply
45	VSSPP	I	Negative power supply
46	BP0	O	Push Pull output 1
47	VDDPP	I	Positive power supply
48	BN0	O	Push Pull output 2
49	VSSPP	I	Negative power supply

Working Voltage Range：

The chip is designed for supporting wide operation voltage from 2.4V to 5.1V that is suitable for 2 batteries (2.4V ~ 3.6V) or 3 batteries operated (2.7V ~ 5.1V) application. To achieve the best performance, it is required to keep the voltage level of CVDD below 3.6V for both 2 or 3 batteries applications.
For 2 batteries application, CVDD can be handled as usual power pins connection (please refer to application note in Chapter 13).

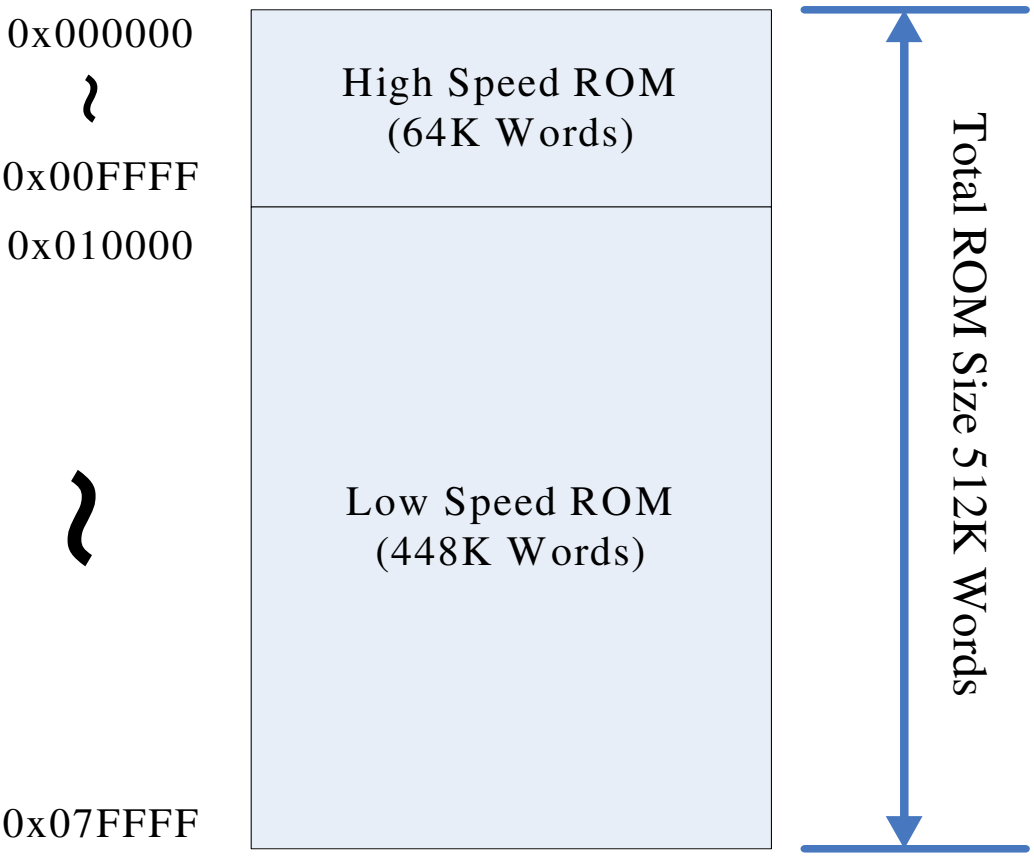
For 3 batteries application, SNC7x9 is designed with internal voltage regulation for CVDD which is connected to the REG_OUT (please refer to application note in Chapter 13)

Below is the operation voltage range for each power pins. See chapter 10 for regulator detail and chapter 13 for 2 batteries & 3 batteries application circuit detail

Power Name	Range
CVDD	2.4V ~ 3.6V
VDDA	2.4V ~ 5.1V
VDDIO0	2.4V ~ 5.1V
VDDIO1	2.4V ~ 5.1V
VDDIO2	2.4V ~ 5.1V
VDDPP	2.4V ~ 5.1V

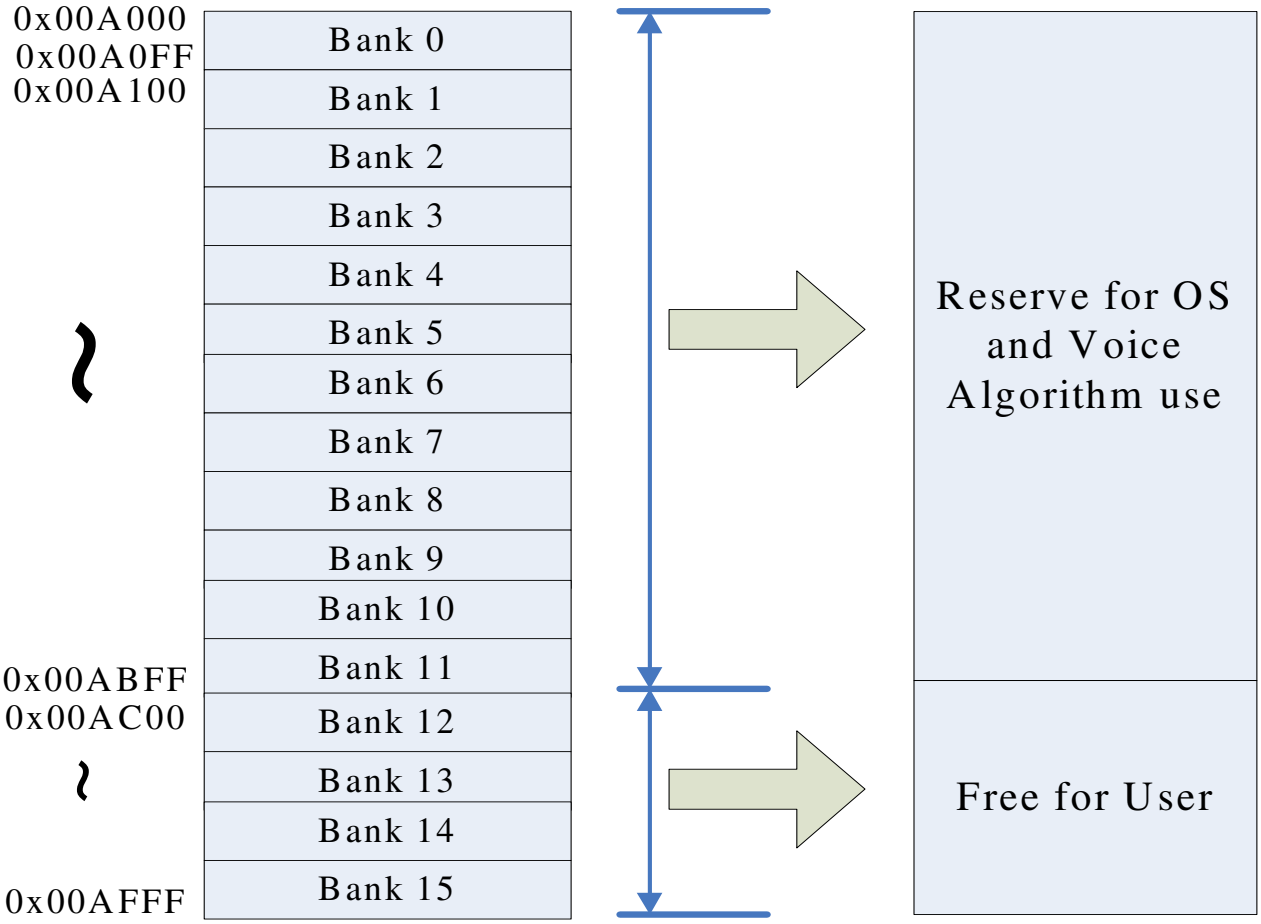
4. ROM TABLE

The total ROM size is 512K words. It split two parts including high speed and low speed ROM area, but user also can program all area. In high speed ROM had a small OS to control all function flow. We recommend user put you program in high speed ROM and put data in low speed ROM to get high performance.



5. RAM TABLE

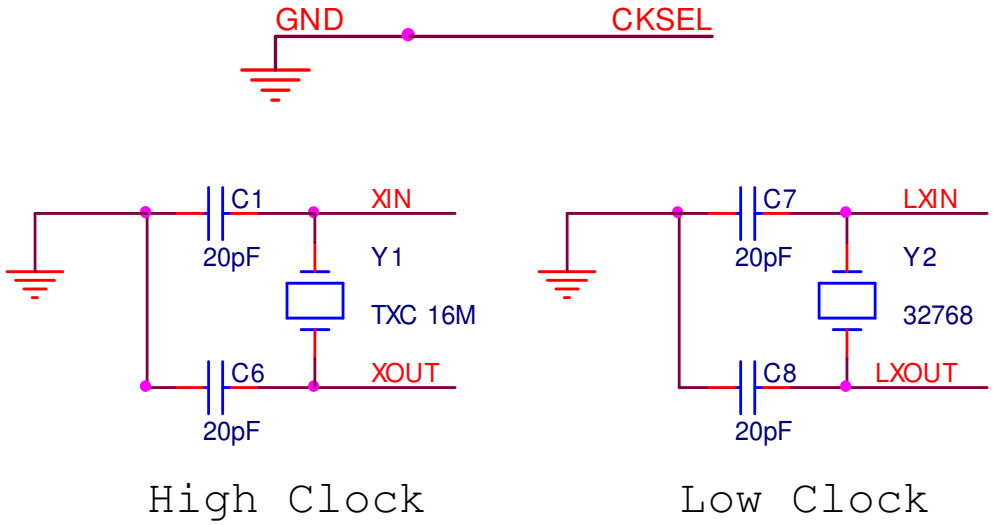
Total RAM size is 4K words, and each one bank is 256 words. The RAM size 0~3K words is for algorithm using and last 1K words is for user using.



6. System Clock

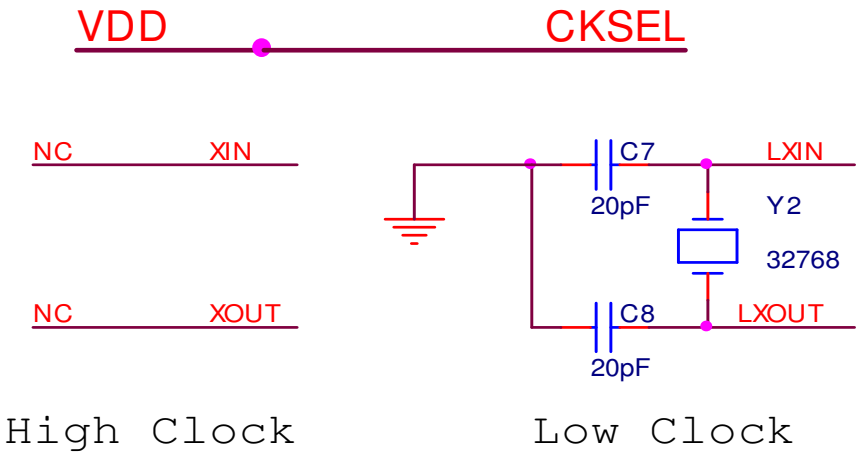
The system clock had dual source high clock and low clock input, user can selected from 16Mhz crystal or ROSC for high clock and 32768 crystal for low clock. In Normal mode, user can select high clock source from 16Mhz crystal or ROSC, In Slow mode, user must select 32768 crystal to input system clock.

6.1 Crystal Input



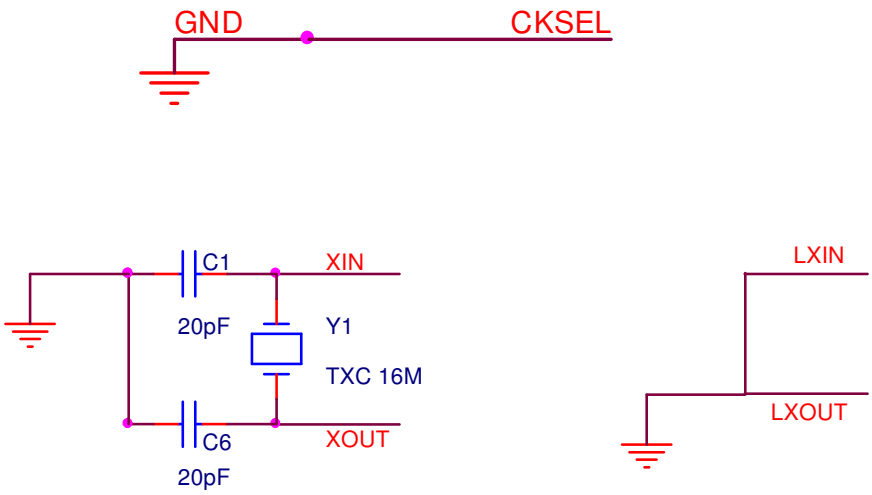
6.2 ROSC Input

User uses ROSC mode to make High clock. The internal clock is reference clock from 32768 X'tal to fine tune to 16MHz. ***In order to get an accurate system clock by ROSC, the real time clock source is recommended to connect a 32768HZ crystal for system clock calibration.***



6.3 Crystal Input without 32768 crystal

Product use “Crystal input” and without “Low clock (slow mode)” application, please connect the LXIN and LXOUT pins to **ground**.



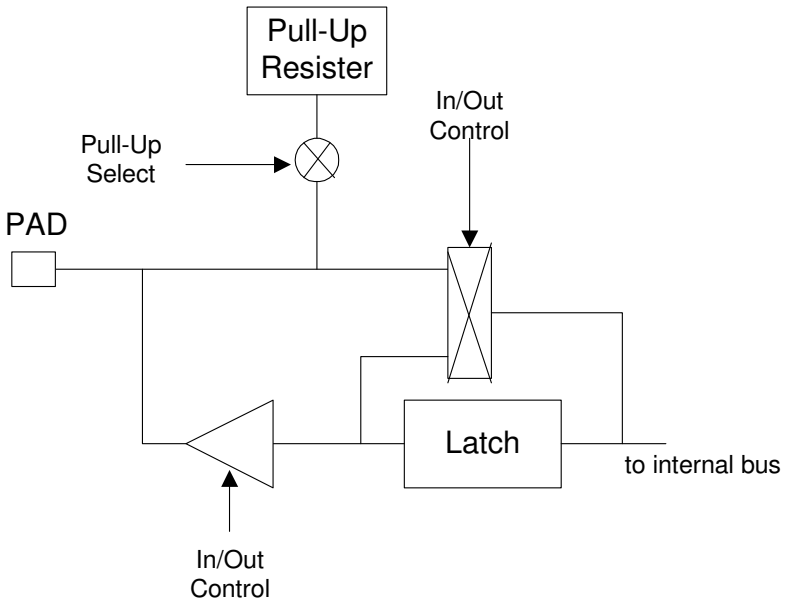
High Clock Low Clock

7. I/O PORT

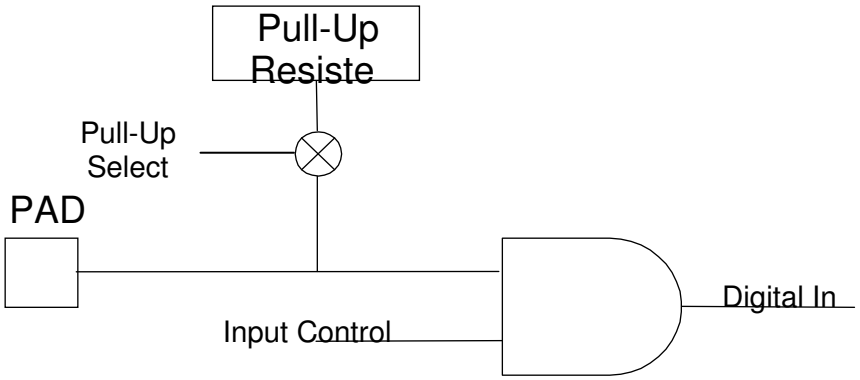
SNC749 provides one a 24-bit I/O port for user application (P0.0~P0.15, P1.0~P1.7). The input pull high resistor of each pin can be programmed by Port Pull-High register. The direction of I/O port is selected by Port Direction register.

The Port0 (P0.0~P0.15) and Port1 (P1.0~P1.7) can wake the chip up from the stop mode and watch mode. P0.15 can be modulated with a 38.5Khz carry signal to realize IR signal transmission.

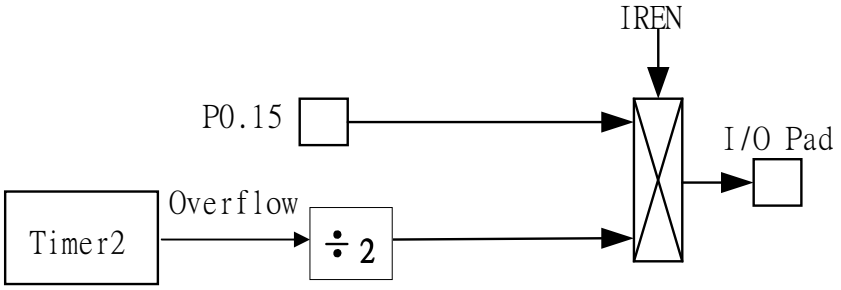
When user uses GPIO to wake up chip, the GPIO must setting to input mode and Pull-High all I/O pin.



I/O Configuration of P0.0~P0.15



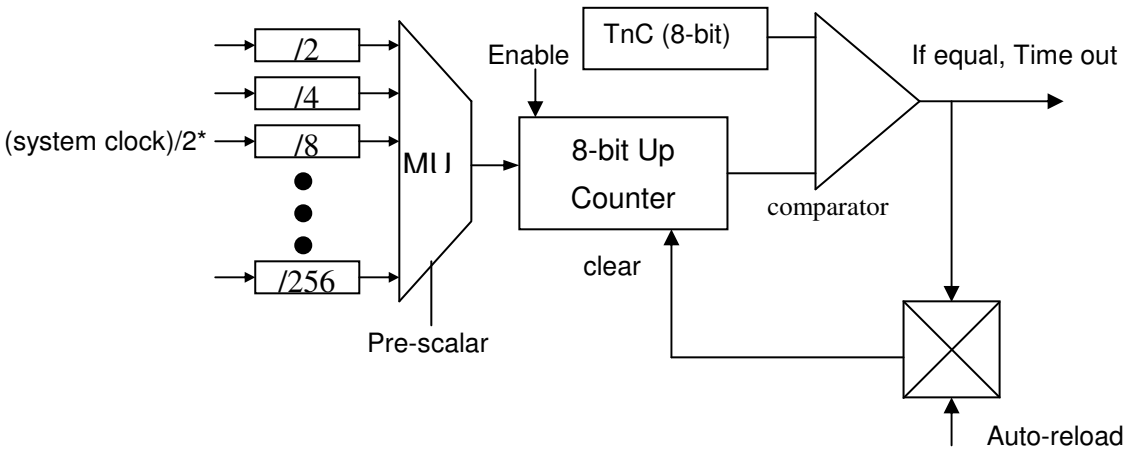
Input Port Configuration of Port 1 (P1.0~P1.7)



P0.15 Modulated with a carry signal

8. TIMER/COUNTER

SNC749 provides three 8-bit timer/event counters (T0/T1/T2). Each timer is 8-bit binary up-count timer with pre-scalar and auto-reload function. Timer 0 (T0) is used when voice playing, so user should avoid to use T0.



9. Push-Pull DAC

To play out voices, SNC749 only contains Push-Pull DAC (direct drive) for user to output voice.

10. Regulator

The SNC749 provide a linear regulator for core power (CVDD). The accuracy output voltage is 2.8V±0.2V and it can be power-downed by software. It is an internal regulator, user doesn't need use external regulator to provide 3.3 voltages for core power (CVDD).

Features:

Input supply voltage: 2.7V ~ 5.1V

Output current: 20mA

Accuracy output voltage: 2.6~3.0V

11. ABSOLUTE MAXIMUM RATINGS

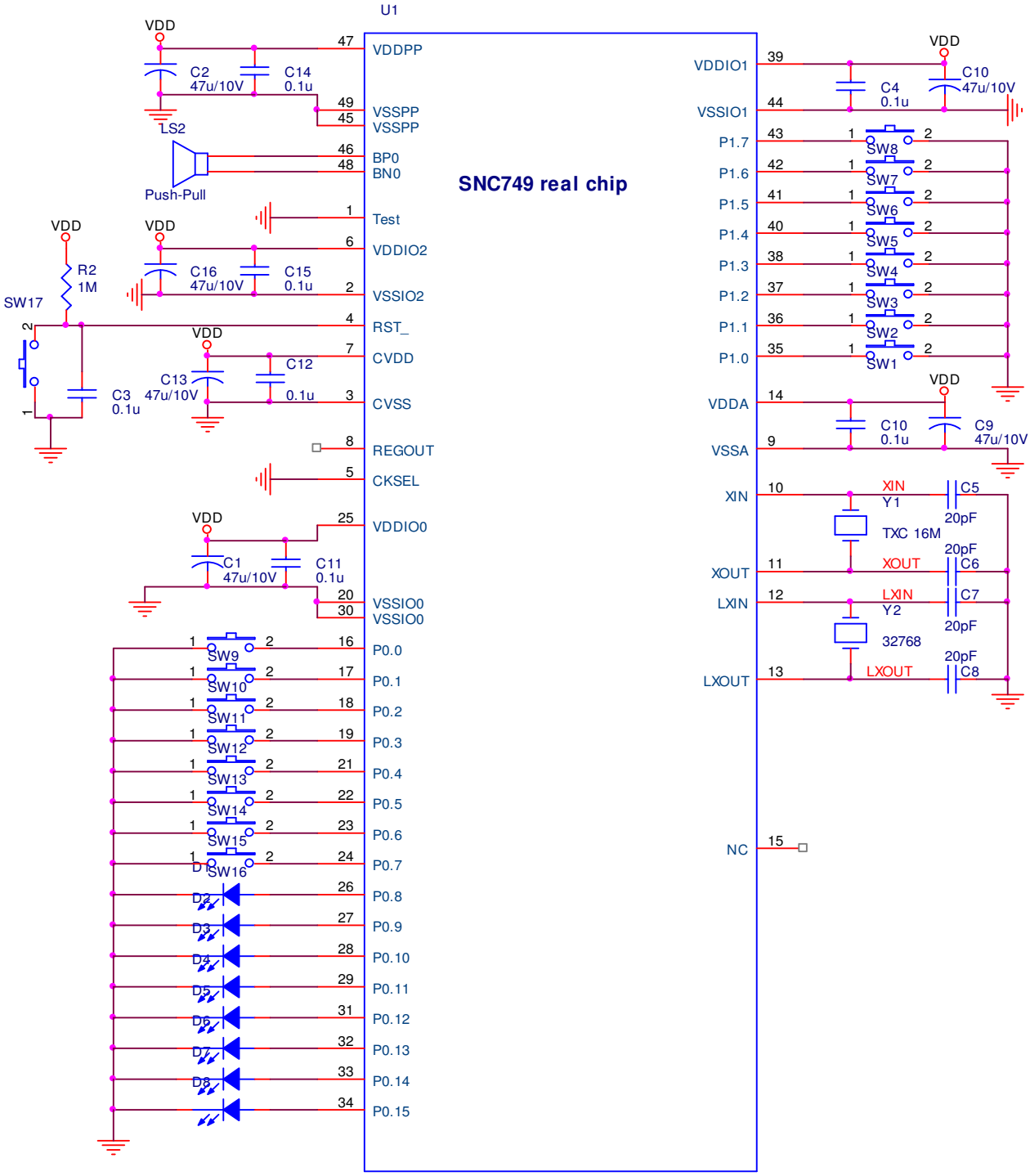
Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	6.0	V
Input Voltage	V_{IN}	GND-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55	°C
Storage Temperature	T_{STG}	-55.0	125.0	°C

12. ELECTRICAL CHARACTERISTICS

Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	-	5.1	V	
Standby current	I_{SBY}	-	2.0	-	*u*A	V_{DD}=3V, no load
Operating Current	I_{OPR}	-	10	-	mA	V_{DD}=3V, no load
Watch mode Current	I_{WCH}	-	12	-	uA	V_{DD}=3V,9instructions
Slow mode Current	I_{SL}	-	200	-	uA	V_{DD}=3.3V, no load
Pull-Up resistor of P0, P1	R_{PU}	-	800	-	KΩ	V_{DD}=3V, no load
Input current of P0, P1	I_{IH}	-	-	10.0	*u*A	V_{DD}=3V,V_{IN}=3V
Drive current of P0, P1	I_{OD}	-	4	-	*m*A	V_{DD}=3V,V_O=2.4V
Sink Current of P0, P1	I_{OS}	-	6	-	*m*A	V_{DD}=3V,V_O=0.4V
Drive current of Buo1	I_{OD}		150	-	*m*A	V_{DD}=3V,Buo1=1.5V
Sink Current of Buo1	I_{OS}		150	-	mA	V_{DD}=3V,Buo1=1.5V
Drive Current of Buo2	I_{OD}		150	-	mA	V_{DD}=3V,Buo2=1.5V
Sink Current of Buo2	I_{OS}		150	-	mA	V_{DD}=3V,Buo2=1.5V
Oscillation Freq. (crystal)	F_{OSC}	-	16.0	-	MHz	V_{DD}=3V

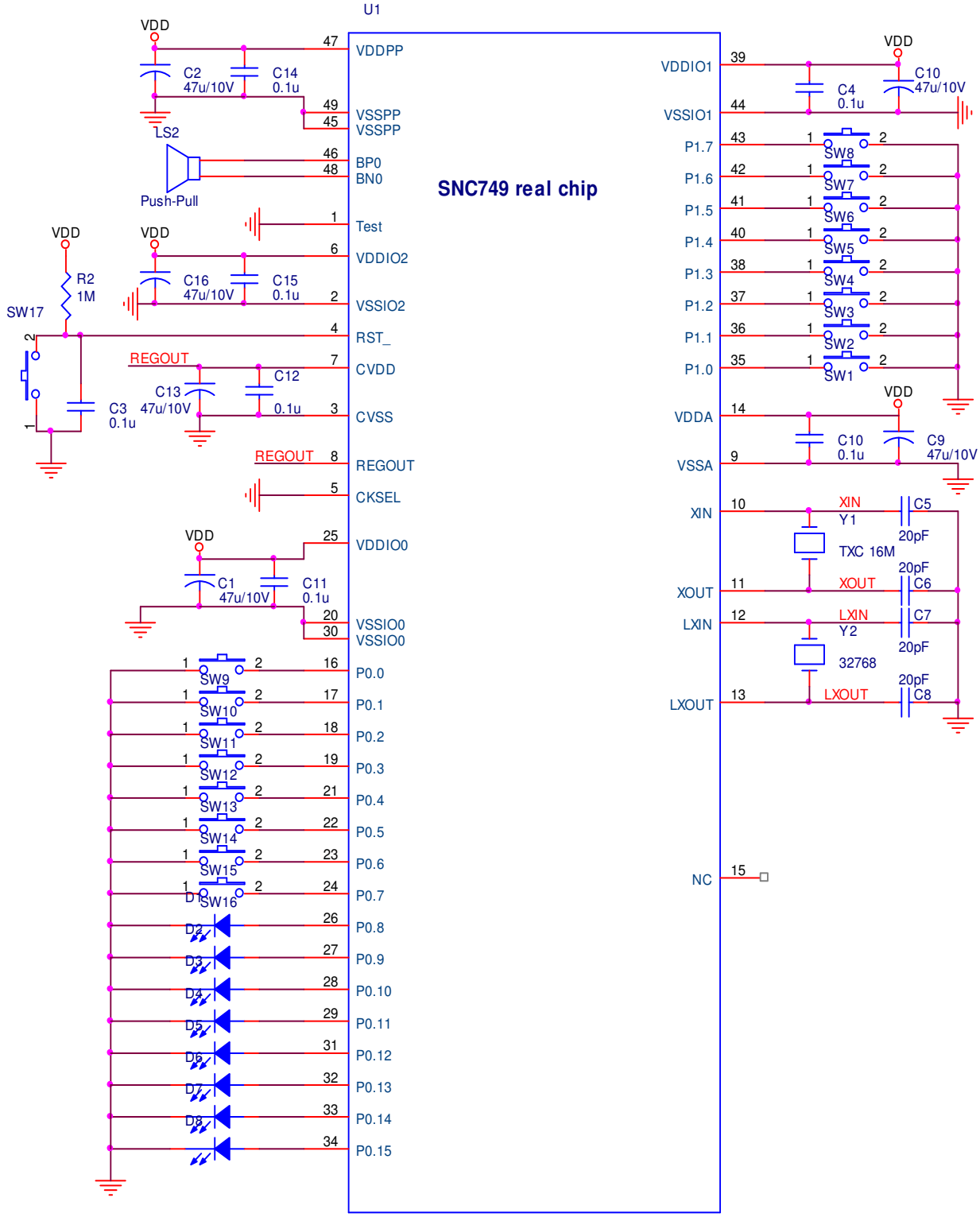
13. Application Circuit

X'TAL (Use 2 battery, VDD = 2.4V ~ 3.6V)



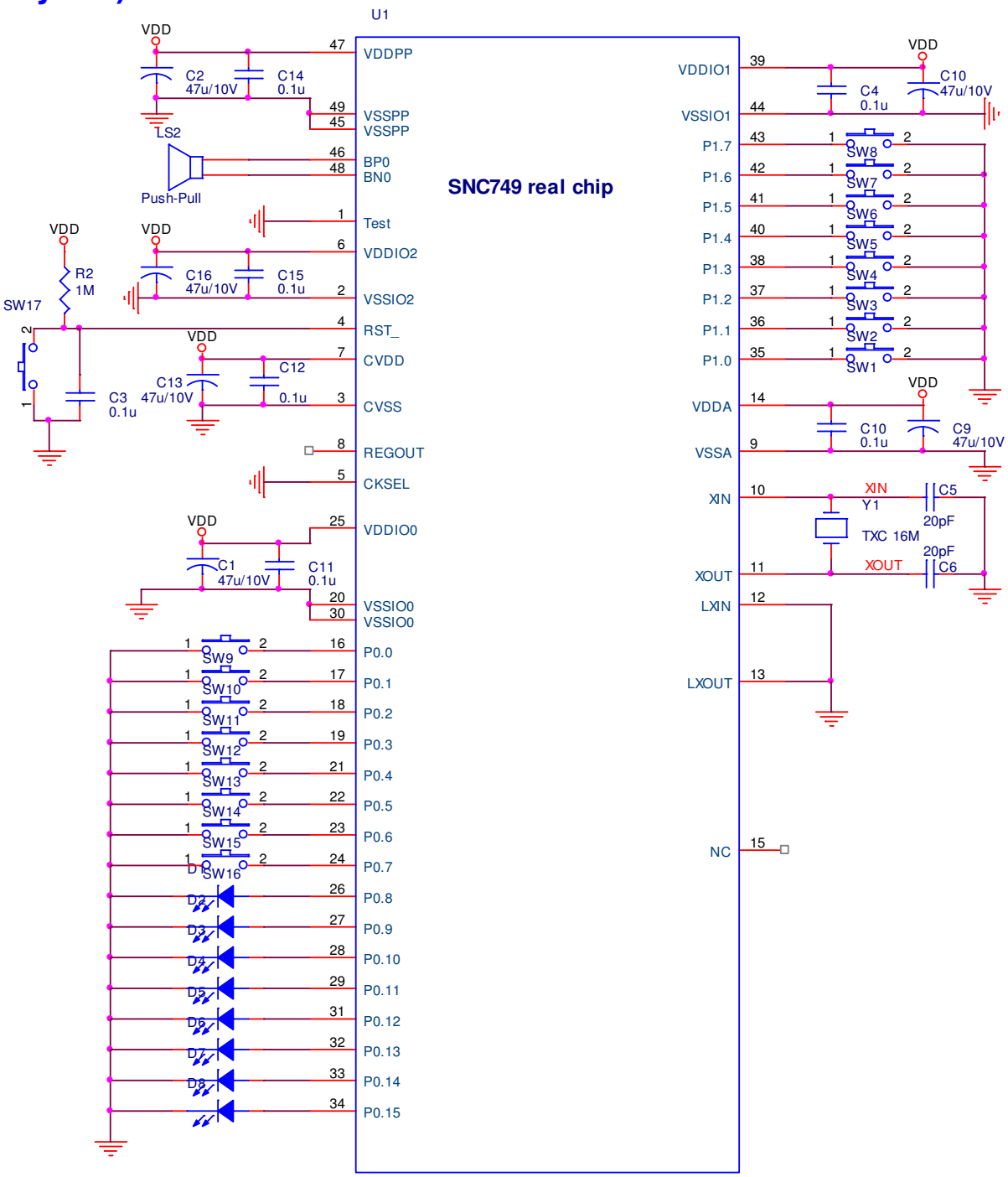
Note: The SNC749 total have 6 powers, each power use one 47uF and one 0.1uF capacitor. If user wants to save cost, you can use 0.1uF on each power and add 47uF on VDDPP and VDDA.

X'TAL (Use 3 battery, VDD = 2.7V ~ 5.1V)



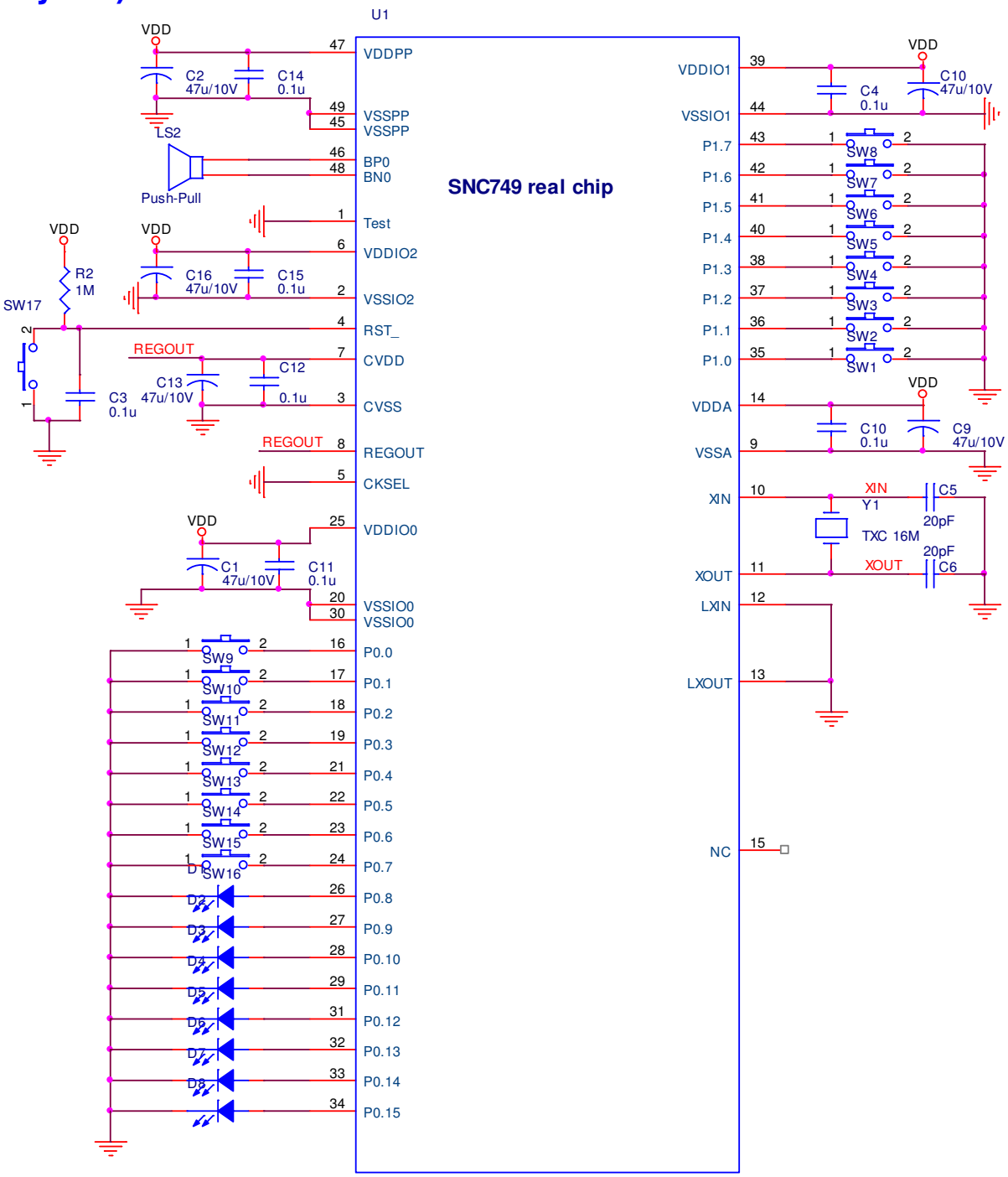
Note: The SNC749 total have 6 powers, each power use one 47uF and one 0.1uF capacitor. If user wants to save cost, you can use 0.1uF on each power and add 47uF on VDDPP and VDDA.

X'TAL (Use 2 battery, VDD = 2.4V ~ 3.6V, without 32768 crystal)



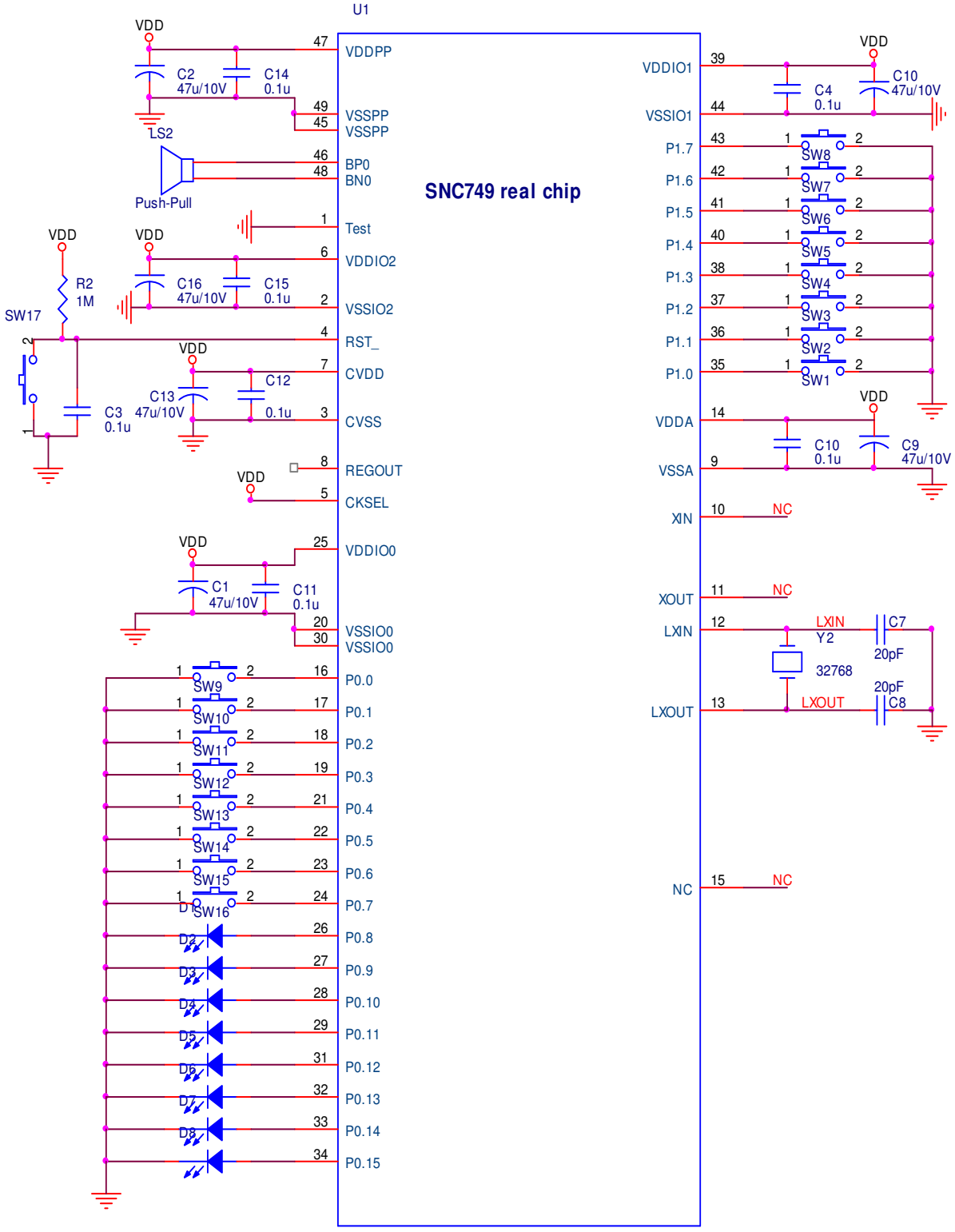
Note: If application doesn't 32768 crystal, please connect the LXIN and LXOUT to **ground**, it might cause 1~2uA at each pin at 3V.

X'TAL (Use 3 battery, VDD = 2.7V ~ 5.1V, without 32768 crystal)



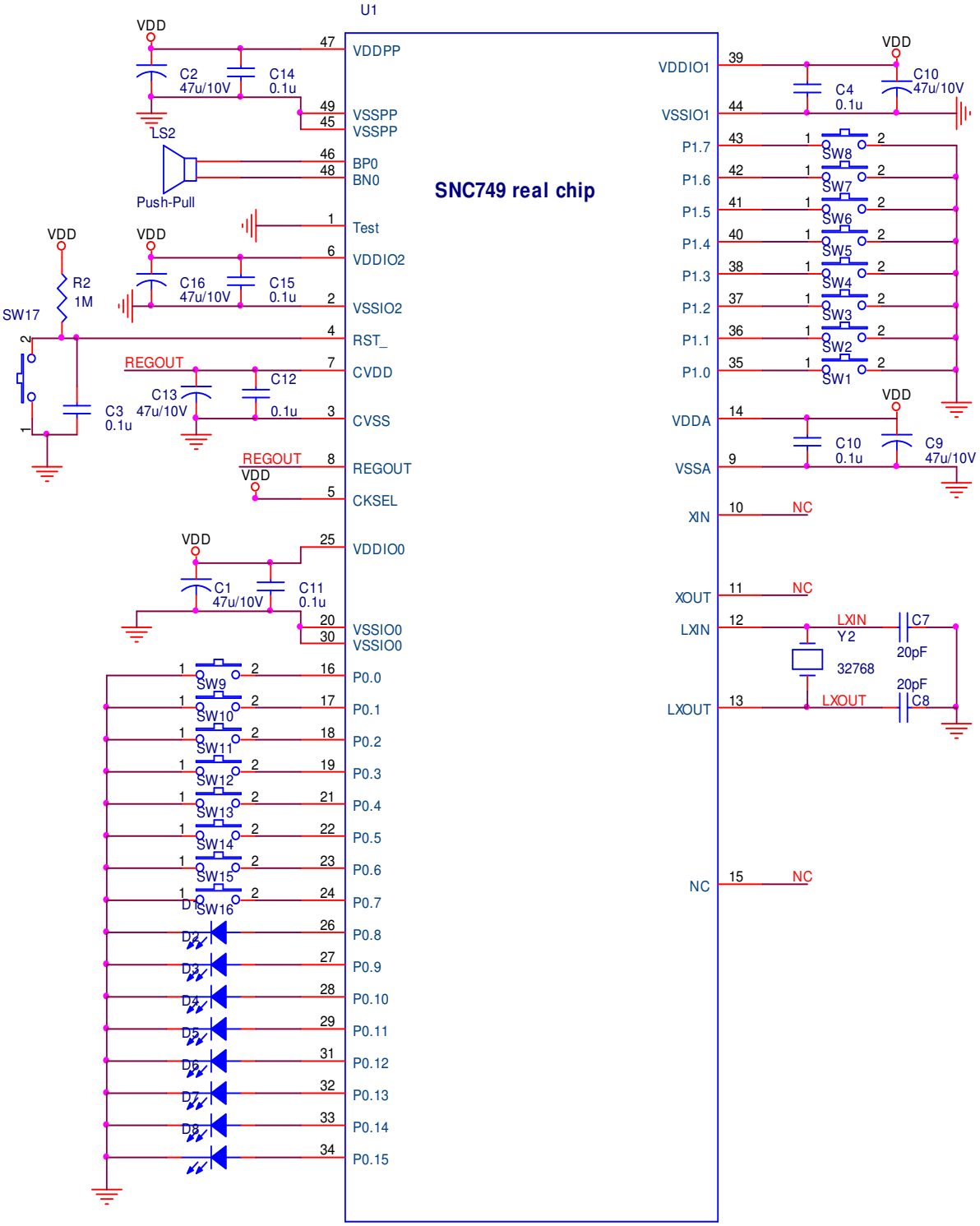
Note: If application doesn't 32768 crystal, please connect the LXIN and LXOUT to **ground**, it might cause 2~3uA at each pin at 4.5V.

ROSC (Use 2 battery, VDD = 2.4V ~ 3.6V)
(Low clock use 32768 x'tal)



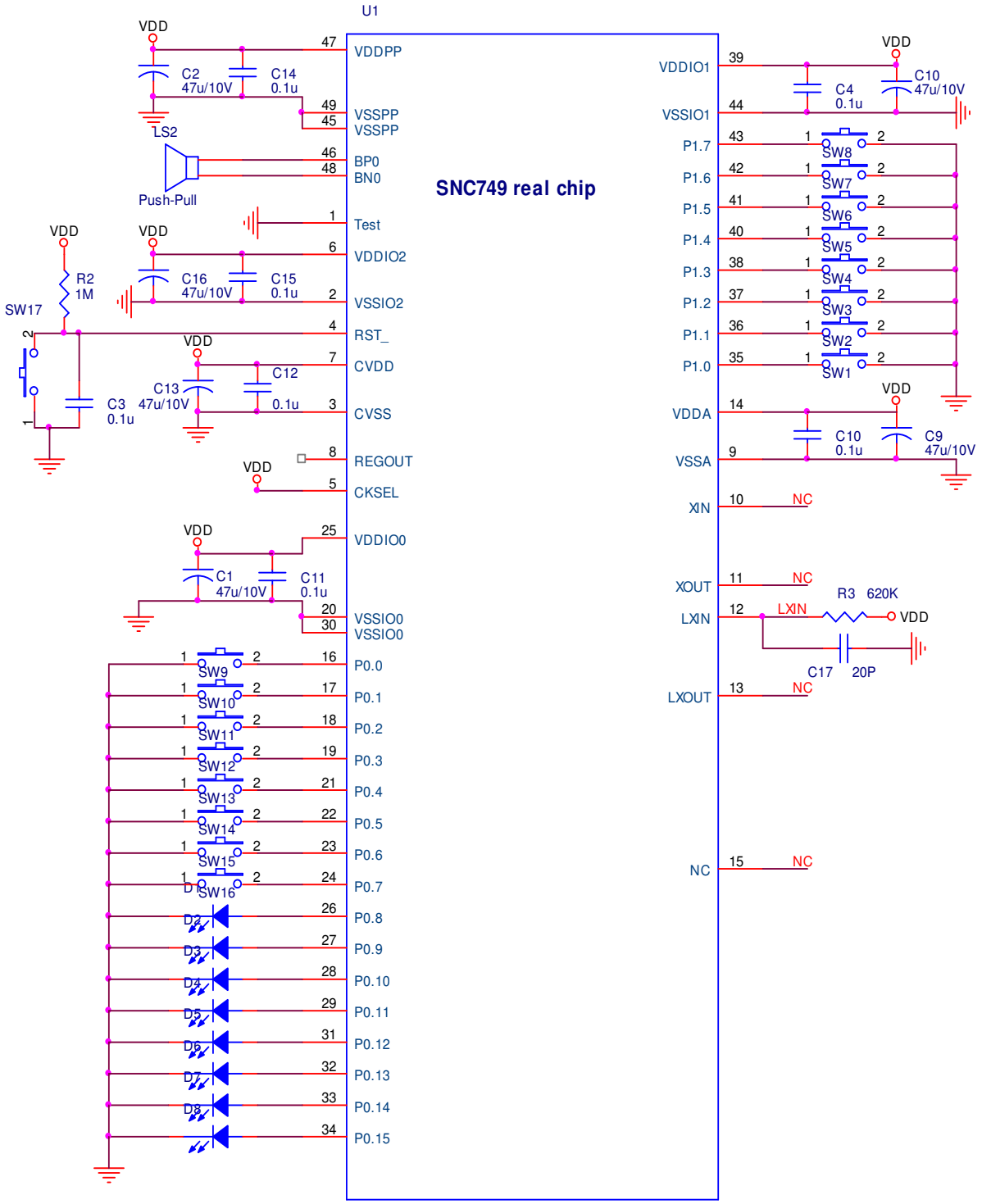
Note: The SNC749 total have 6 powers, each power use one 47uF and one 0.1uF capacitor. If user wants to save cost, you can use 0.1uF on each power and add 47uF on VDDPP and VDDA.

ROSC (Use 3 battery, VDD = 2.7V ~ 5.1V)
(Low clock use 32768 x'tal)



Note: The SNC749 total have 6 powers, each power use one 47uF and one 0.1uF capacitor. If user wants to save cost, you can use 0.1uF on each power and add 47uF on VDDPP and VDDA.

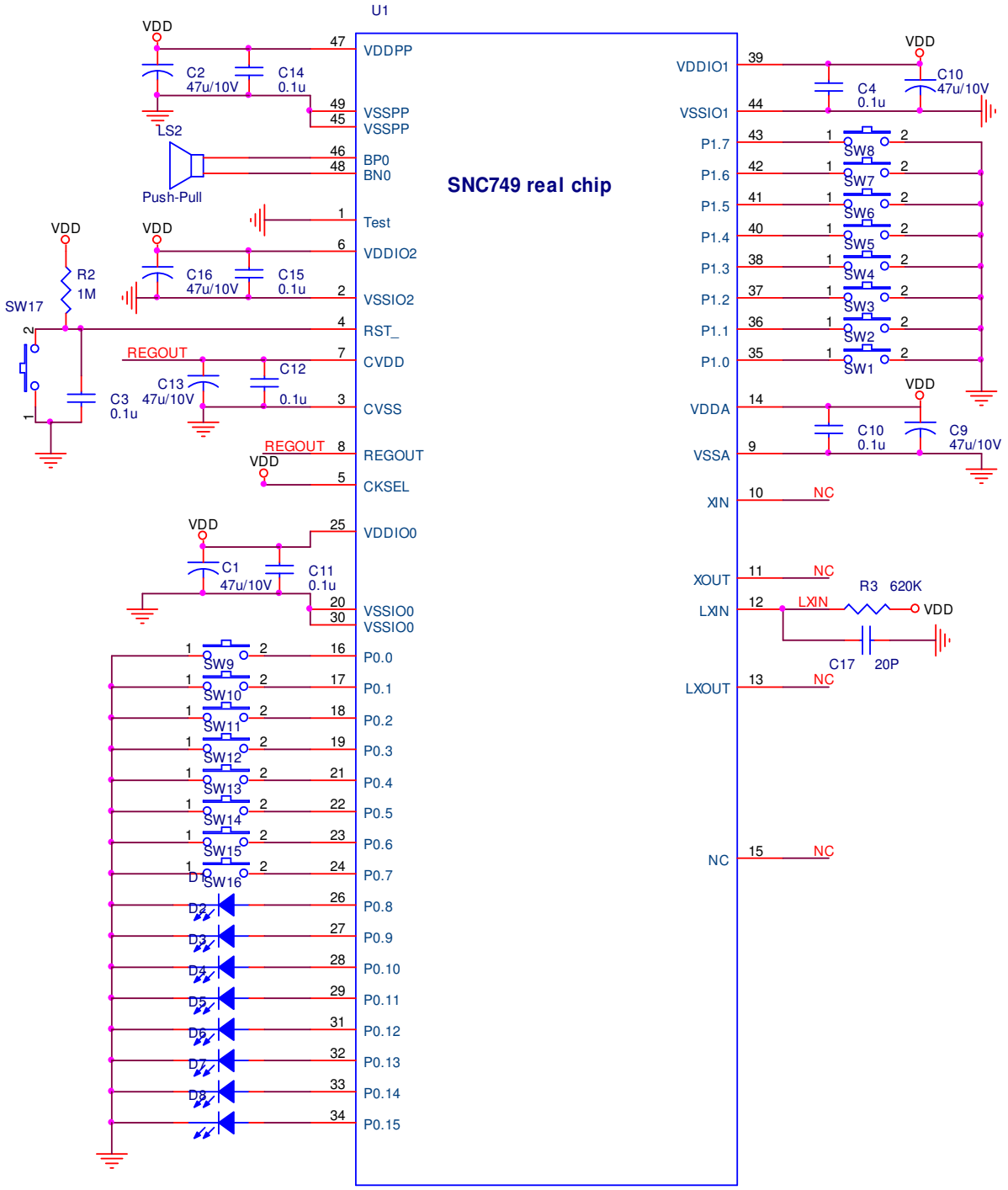
ROSC (Use 2 battery, VDD = 2.4V ~ 3.6V)
(Low clock use resister)



Note: 1. The SNC749 total have 6 powers, each power use one 47uF and one 0.1uF capacitor. If user wants to save cost, you can use 0.1uF on each power and add 47uF on VDDPP and VDDA.

2. If user choice this resolution, please reference programming guide about Low Clock Input Select chapter.

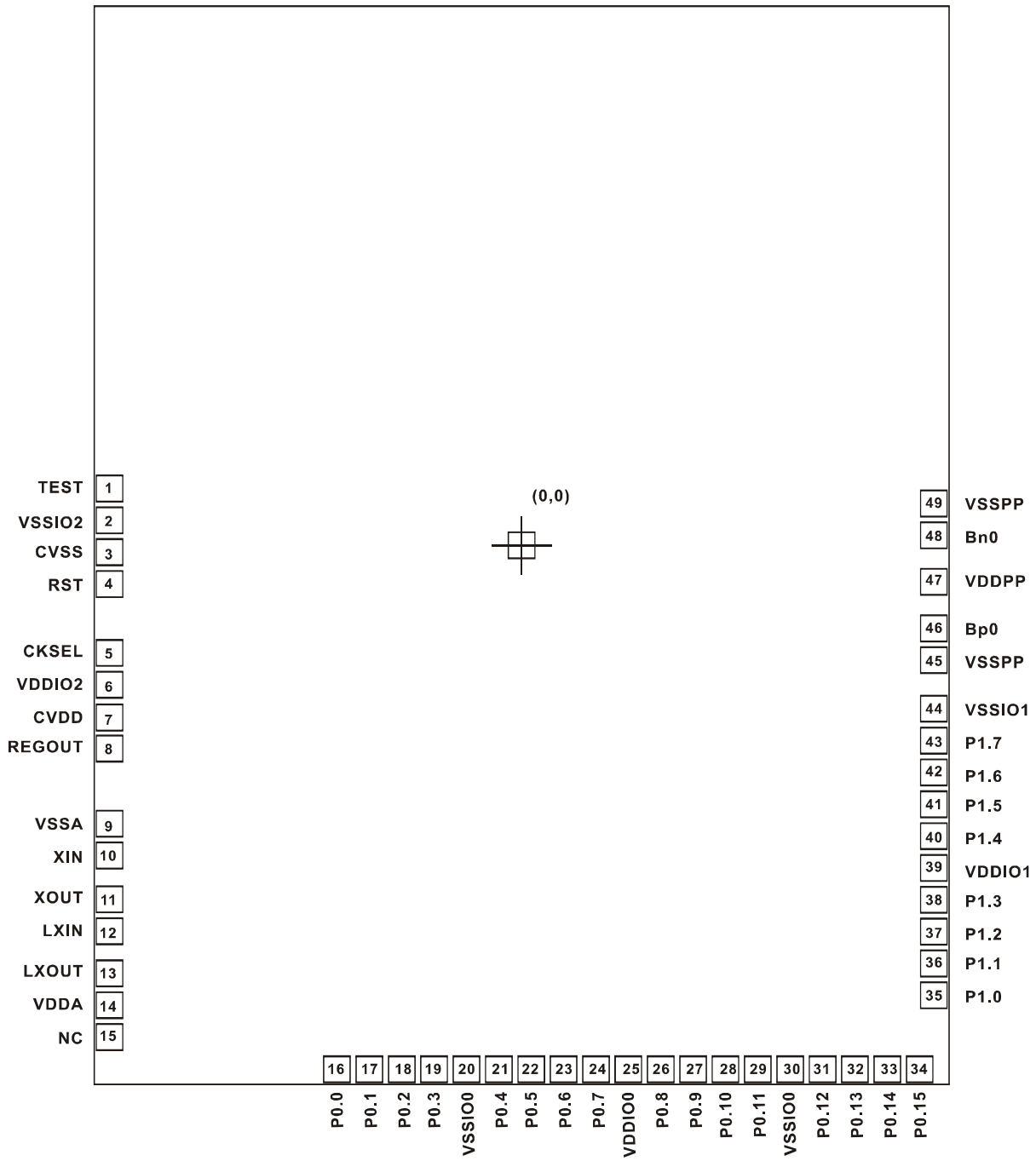
ROSC (Use 3 battery, VDD = 2.7V ~ 5.1V) (Low clock use resister)



Note: 1. The SNC749 total have 6 powers, each power use one 47uF and one 0.1uF capacitor. If user wants to save cost, you can use 0.1uF on each power and add 47uF on VDDPP and VDDA.

2. If user choice this resolution, please reference programming guide about Low Clock Input Select chapter.

14. Bonding PAD



Note： The Substrate must be connected to **GND** in PCB layout.

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