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AMENDENT HISTORY

Version	Date	Description
Ver 1.0	2007/11/27	First Release
Ver 1.1	2008/1/18	Modify on voice algorithm library & USB interface
Ver 1.2	2008/3/5	Modify Application Circuit
Ver 1.3	2008/8/22	Correct Application Circuit with USB
Ver 1.4	2009/3/19	Correct Application Music Player

1. INTRODUCTION

The SNC715 is a high performance 16-bit DSP base processor with 16MIPS CPU power. The internal 32K words hi-speed ROM already built-in a hi-performance software voice synthesizer to provides lot of voice hi-decompression libraries which can support from 16kbps ~ 96kbps compression rate for speech and music. SNC715 also built-in a Low Voltage Detector circuit for power management and a USB 1.1 interface for communication with PC.

2. FEATURES

- Power supply:
  2.4V ~ 3.6V (for 2 batteries application)
  3.6V ~ 5.1V (for 3 batteries application)
- Built-in regulator for DSP core
- Built-in 16-bit DSP core
- Software-based voice/melody processing
- Rich Function Instruction Set
- 16 MIPS CPU performances under 16MHz
- Clock system
  - 6MHZ crystal for hi-speed system clock
  - 32768HZ crystal oscillator for RTC and low-speed system clock
- 6 Interrupt Sources
  - 5 internal interrupt (T0, T1, T2, RTC and USB)
  - 1 DA interrupt
- I/O Ports: 16 I/O pins (P1.0~P1.15)
- ROM size: 32K*16 bits
- RAM size: 2K*16 bits
- Three 8-bit timers with auto-reload function (T0, T1, T2)
- Programmable watchdog timer
- Built in PWM direct drive circuit output
- Sampling Rate: 16KHz
- Built-in software voice synthesizer for multiple bit-rate solution
- USB 1.1 interface provided (Mass Storage Class)
- Low Voltage Detector
- Low Voltage Reset

3. PIN ASSIGNMENTS

Symbol	Descriptions	No. of PIn	Pin Count
VDDA	Power for OSC	1	1
VDDPWM	Power for PWM	2	3
VDDIO1	Power for Regulator	1	4
VDDIO2	Power for port1	1	5
VSSA	GND for OSC	1	6
VSSPWM	GND for PWM	2	8
VSSIO	GND for IO	2	10
VDDC	Power + for core	2	12
VSSC	Power - for core	2	14
VREG	Regulator voltage output	1	15
XIN	High speed clock crystal input	1	16
XOUT	High speed clock crystal output	1	17
LXIN	Low speed clock crystal input	1	18
LXOUT	Low speed clock crystal output	1	19
BUO1	PWM output	1	20
BUO2	PWM output	1	21
RST_	Chip reset	1	22
TEST	For test only	1	23
D+	USB Data +	1	24
D-	USB Data -	1	25
VDDUSB	USB power +	1	26
VSSUSB	USB power -	1	27
P1.0~P1.15	General I/O port P1.0~P1.15	16	43

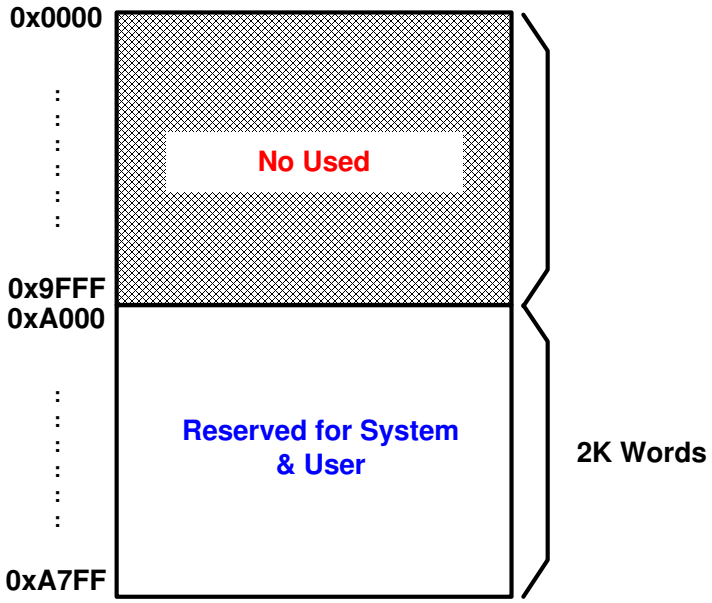
4. MEMORY

4.1 Internal ROM

SNC715 provides hi-compression algorithm to compress voice data in order to save more memory size. So all the de-compression program has be built at the internal ROM of SNC715 and system will reserved some necessary ROM space for those de-compression program automatically once user active the de-compression function. There are totally 32K words of SNC715 internal ROM, user can built-in his own program in the internal ROM for his application except necessary space for de-compression program.

4.2 Internal RAM

The internal totally 2K words RAM and the SRAM regions 0xA000~0xA7FF are reserved for system and user's application.



5. Clock System

SNC715 is a dual clock system that it provides high-speed clock (16MHz) and low-speed clock (32768Hz).

5.1 Normal Mode

The normal mode means CPU main clock source comes from hi-speed clock, so SNC715 is run in full speed. The hi-speed clock source is through external 6MHz pumping to 16MHZ by the internal PLL circuit.

5.2 Low-speed mode

This is a special operation mode of SNC715, the hi-speed clock is disabled and main clock of SNC715 comes from low-speed clock source (32768Hz). It will save much power consumption when chip works on the low-speed mode.

5.3 Stop Mode

In stop mode, all the system clocks are stop (16MHz & 32768Hz) and chip entry a very low power consumption state. Chip will wake-up from stop mode once any IO state change or external interrupt occurs.

5.4 Watch Mode

This mode is for some real time clock application, users have to add a 32768Hz crystal to realize RTC function. Considering to saving power consumption, user should stop the hi-speed clock source (16MHZ) and enable the low-speed clock source. Then chip will entry power down mode but the low-speed clock still working and wake-up chip when the RTC period is happened in order to fresh the RTC timer.

There are three options for RTC interrupt periods, users can select 0.25sec/0.5sec and 1sec through the RTC control register.

If chip is in power-down mode and interrupt enable is active for RTC, then chip will be wake-up from power-down mode per 0.25/0.5/1 second.

6. POWER ON RESET

When “L” level appears on RESET PIN, the chip will enter RESET state.

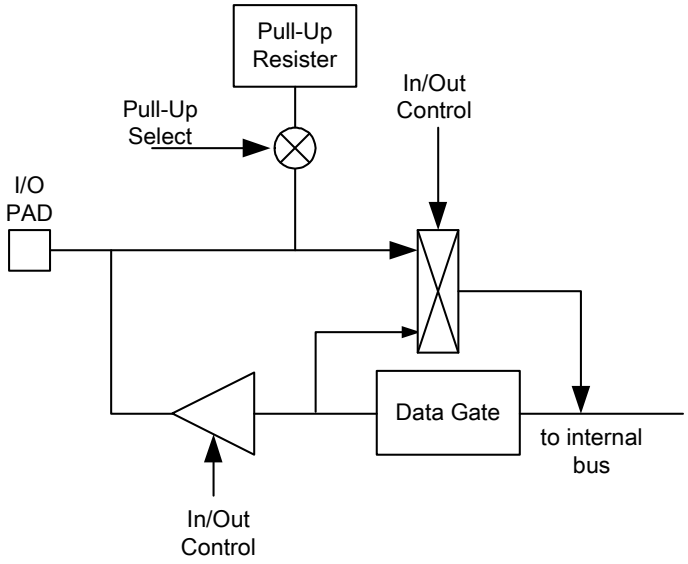
After reset, the chip does not execute the first instruction until counting 2^{17} clock cycles. It takes around 8.2ms at 16MHz. (crystal for clock source), and the location of the first instruction after RESET is 0x000000. In additional, all the contents of SRAM will be unchanged during RESET stage.

Note: All the contents of SRAM data will be set to 0x00 after reset.

7. I/O PORT

SNC715 provides totally 16 I/O pins (P1.0~P1.15). The input pull-high resistor of each pin can be programmed by port pull-high register and the direction of I/O port is selected by port direction register. The I/O port P1.0~P1.15 can wake the chip up from the stop mode and watch mode.

The internal structure of I/O pins is showed in **Figure-1**.



I/O Configuration of Port1

Figure-1

8. TIMER/COUNTER

SNC715 provides three 8-bit timer/event counters (T0/T1/T2). Each timer is 8-bit binary up-count timer with pre-scalar and auto-reload function. Timer 0 (T0) was used when voice playing, so user should avoid to use T0.

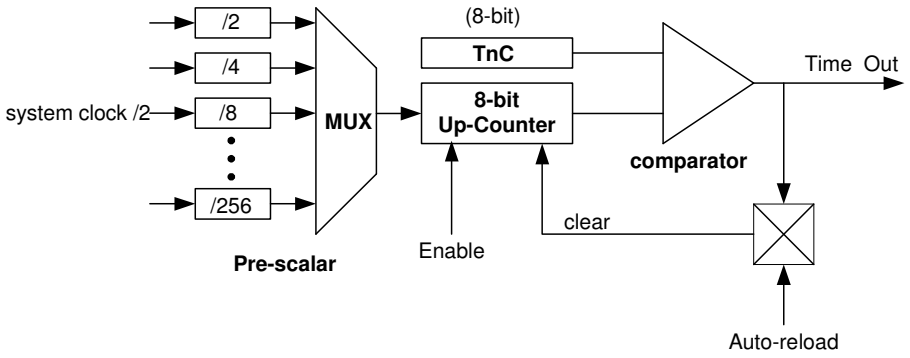


Figure-2

9. PWM

A PWM Direct Drive circuit is built-in SNC715. The maximum resolution of PWM is 11 bits. Two huge output stage circuits are designed in SNC715. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.

10. Low Voltage Detector

SNC715 built in a low voltage detector for power management. It provides four different detect level, 2.3V, 2.5V, 2.8V and 3.1V. User can set an expect detect level through the PCR control register and polling the acknowledge bit to get the current power level is higher or lower then the detect level. Each detect level is designed by schmitt trigger architecture, that's means each detect level has a detect window.

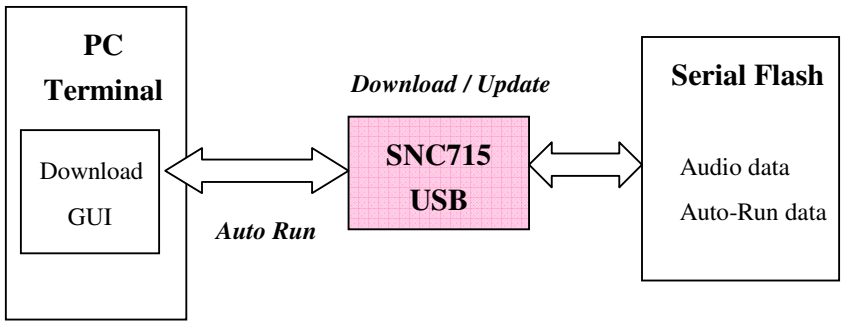
For example, the detect window of detect level 2.3V is 2.24V ~ 2.36V. When the VDD power down below 2.24V, the detect bit of PCR register will be set to 1. Once VDD power is recovered and must be higher then 2.36V, then detect bit is clear by system.

Detect level	Voltage window of schmitt trigger
2.3V	2.24V ~ 2.36V
2.5V	2.44V ~ 2.57V
2.8V	2.72V ~ 2.88V
3.1V	3.01V ~ 3.19V

11. USB INTERFACE

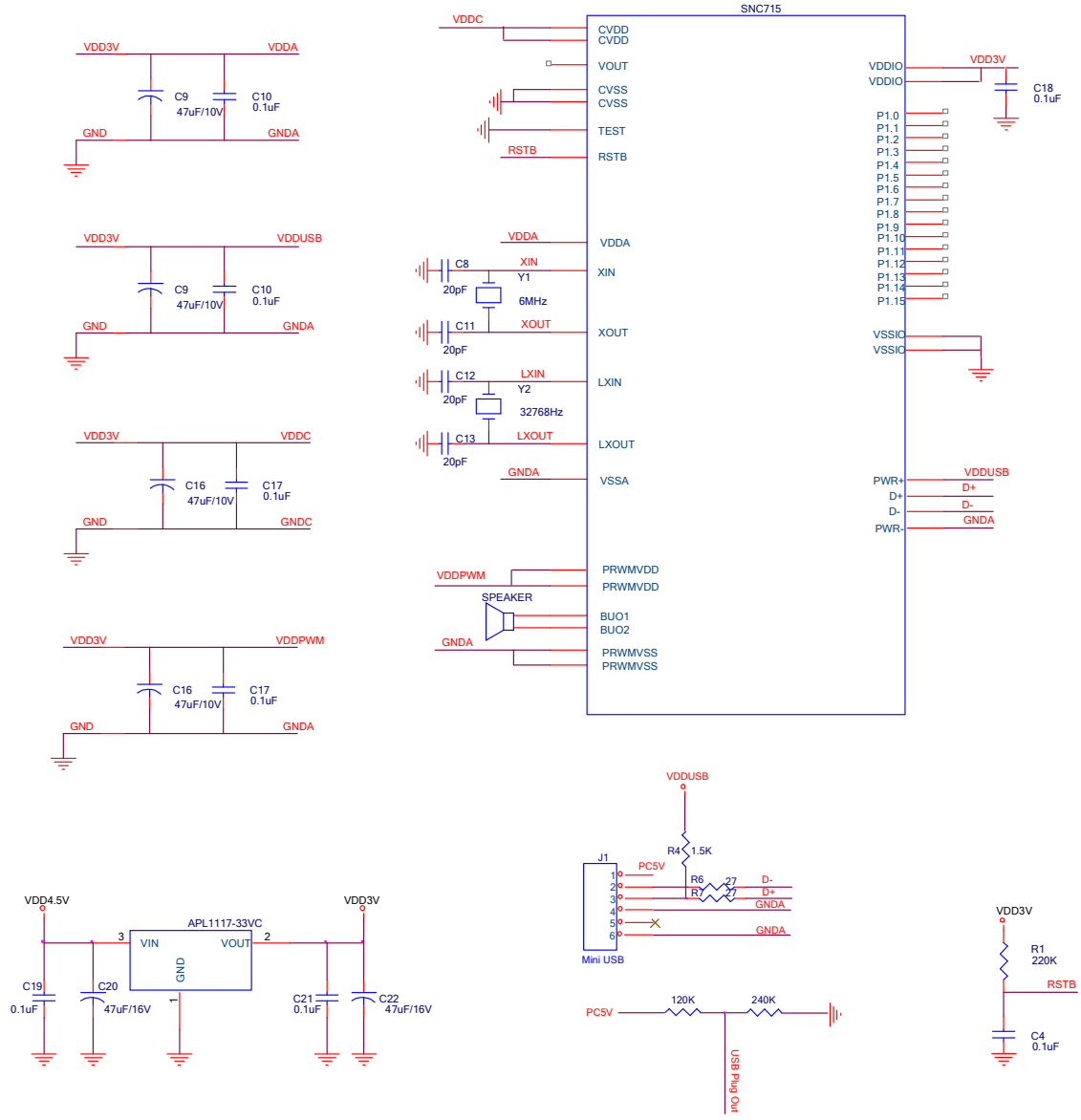
The SNC715 provides a USB 1.1 interface(Mass Storage Class). Users can download/upload data from/to PC through this USB interface.
SNC715 provides twin buffers for data or command transition and the buffer size of those twin buffers is 64bytes each.

SNC715 provides user to do some applications by USB Interface. One is serial flash access, and the other is CDROM Auto-Run function. User can download data to serial flash via USB interface (Under Sonix Download Tool). This function let user can easily extend memory size to store audio data. Another function is Auto-Run. SNC715 USB library can simulate CDROM device to auto run when users plug-in USB.



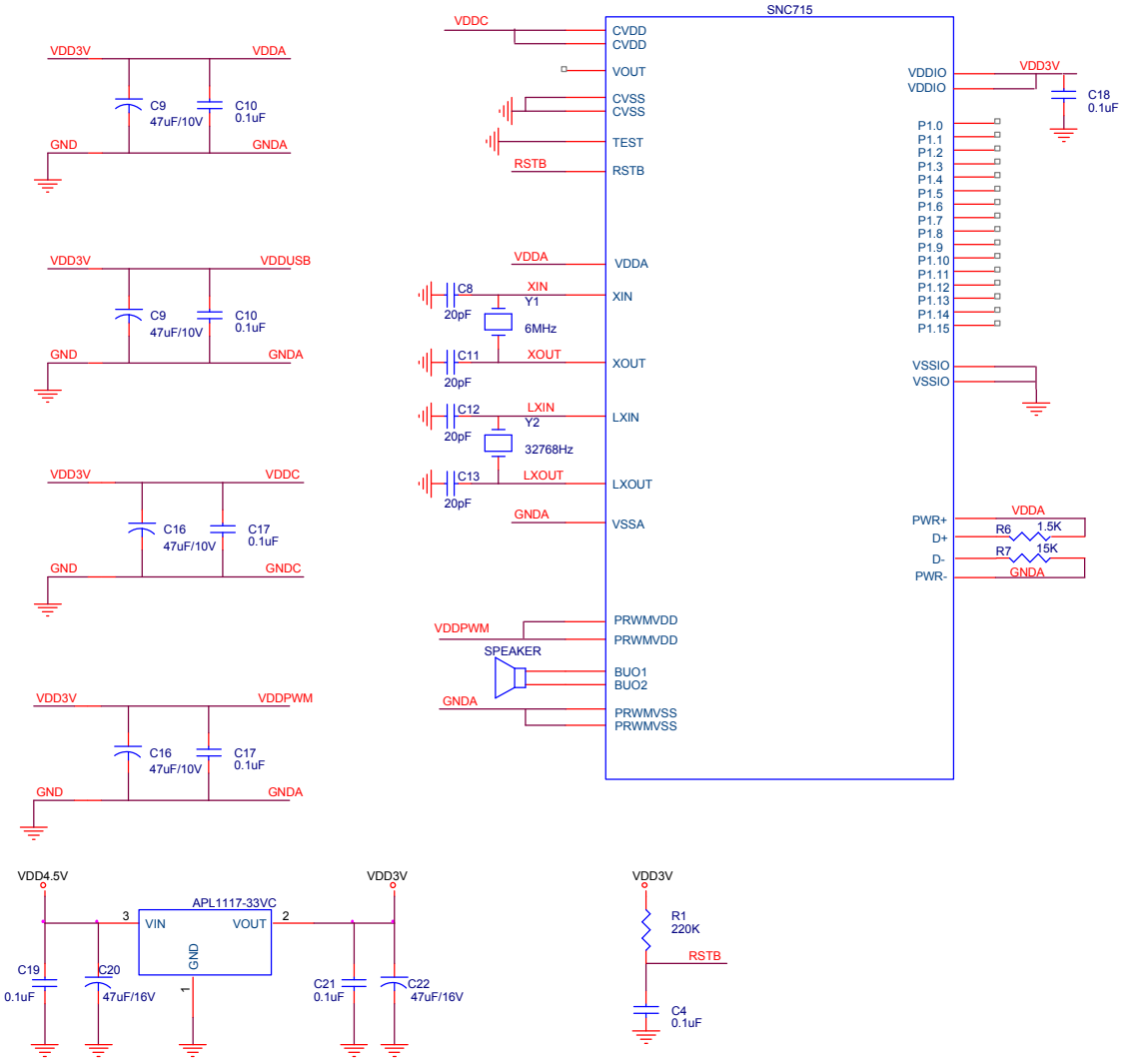
12. APPLICATION CIRCUIT

12.1 Application circuit with USB



Note: The pin 6 of mini USB connect indicate outside 4 pins of mini USB.
Please connect those pins to analog ground.

12.2 Application circuit without USB



Note: If user doesn't need USB function, The D+ pin must connect to 1.5K resistance and pull high, D- pin must connect to 15K resistance and pull low.

13. ABSOLUTE MAXIMUM RATINGS

Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	6.0	V
Input Voltage	V_{IN}	GND-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55	°C
Storage Temperature	T_{STG}	-55.0	125.0	°C

14. ELECTRICAL CHARACTERISTICS

Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	CV_{DD}	2.4	-	3.6	V	
	V_{DD}	3.6	-	5.1	V	
Standby Current Note1	I_{SBY}	-	2.0		uA	V_{DD}=3V, no load
Operating Current	I_{OPR}	-	10		mA	V_{DD}=3V, no load
Pull-Up resistor of P1	R_{PU}	-	800	-	KΩ	V_{DD}=3V, no load
Input current of P1	I_{IH}	-	-	10.0	uA	V_{DD}=3V,V_{IN}=3V
Input Schmitt-trigger window	-	1.5	2.5	-	V	V_{DD}=5V
Drive Current of P1	I_{OD}	-	4	-	mA	V_{DD}=3V,V_O=2.4V
Sink Current of P1	I_{OS}	-	6	-	mA	V_{DD}=3V,V_O=0.4V
Drive Current of Buo1	I_{OD}	360	450	-	mA	V_{DD}=3V,Buo1=1.5V
Sink Current of Buo1	I_{OS}	360	450	-	mA	V_{DD}=3V,Buo1=1.5V
Drive Current of Buo2	I_{OD}	360	450	-	mA	V_{DD}=3V,Buo2=1.5V
Sink Current of Buo2	I_{OS}	360	450	-	mA	V_{DD}=3V,Buo2=1.5V
Oscillation Freq. (crystal)	F_{OSC}	-	6	-	MHz	V_{DD}=3V
Regulator output voltage	VRO	2.6	-	2.8	V	VDD>=3.6V
Regulator supply current	IRS	-	-	20	mA	VOUT=2.6~2.8V
Reset Pin Input Schmitt-Trigger Window		1.68	-	3.81	V	VDD=5V

Note1 : Standby Current : USB Turn Off

15. BONDING PAD

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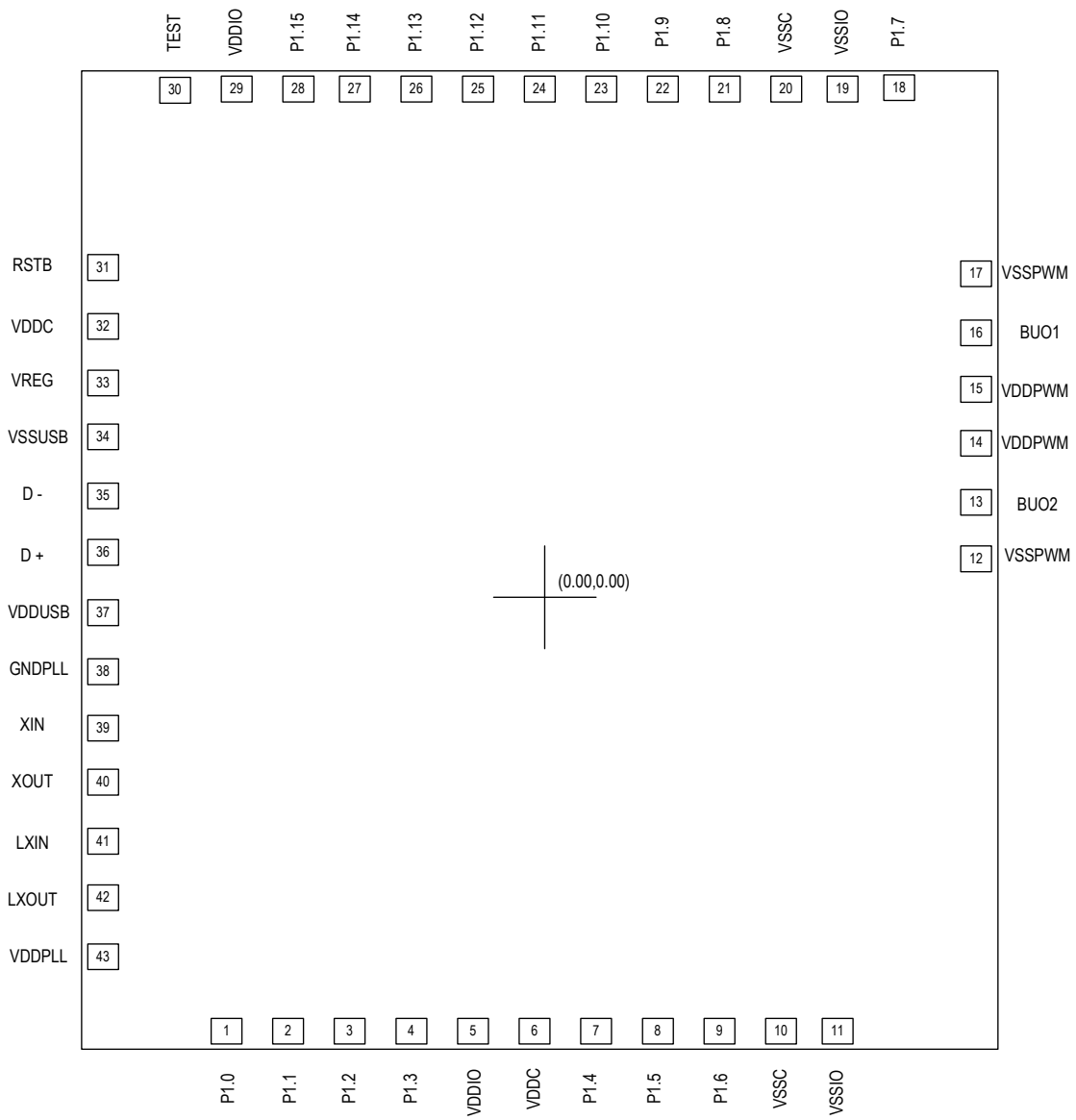
BONDING PAD LOCATION



SNC715

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