======== CONTENTS ========

AMENDENT HISTORY

Version	Date	Description
Ver 1.0	2008/01/22	Formal release
Ver 1.1	2008/02/26	Modify application circuit.
Ver 1.2	2008/03/12	Modify PWM audio output, E-bus description.
Ver 1.3	2008/05/30	Removed Nand flash interface.

1. INTRODUCTION

The SNC712 is a high performance 16-bit DSP base processor with 16MIPS CPU power. The internal 64K words hi-speed ROM already built-in a hi-performance software voice synthesizer to provides lot of voice effects. Such as hi-decompression engine to support from 1.5kbps ~ 32kbps compression rate for speech and music, multi-channel voice synthesizer provides 12-channel wave-table melody, or support foreground 1.5kbps~32kbps and background 4-channel wave-table melody.
The standard microprocessor interface allows SNC712 to extend its memory capability, or connect external device. We also built-in a Low Voltage Detector circuit for power management and a USB 1.1 interface (support mass-storage class) for communication with PC.

2. FEATURES

- Power supply:
  2.4V ~ 3.6V (for 2 batteries application)
  3.6V ~ 5.1V (for 3 batteries application)
- Built-in regulator for DSP core
- Built-in 16-bit DSP core
- Software-based voice/melody processing
- Rich Function Instruction Set
- 16 MIPS CPU performances under 16MHz
- Clock system
  - 6MHZ crystal for hi-speed system clock
  - 32768HZ crystal oscillator for RTC and low-speed system clock
- Extension bus
  - Word-Mode bus interface
  - 3 chip select pins for external devices (such as ROM, Flash, SRAM etc…)
  - Maximum 192M-bit addressing capability
- 9 Interrupt Sources
  - 5 internal interrupt (T0, T1, T2, RTC and USB)
  - 3 external interrupt (P3.0~P3.2)
  - 1 DA interrupt
- I/O Ports: 27 I/O pins (P1.0~P1.15, P3.0~P3.10)
- ROM size: 64K*16 bits
- RAM size: 4k*16 bits
  - 4K*16 SRAM size for general purpose
- Three 8-bit timers with auto-reload function
- Programmable watchdog timer
- Two voice/melody channels or 8 channels wave-table melody
- Built in PWM direct drive circuit output
- Sampling Rate: 8KHz ~16KHz
- Built-in software voice synthesizer for multiple bit-rate solution
- USB 1.1 interface provided
- Low Voltage Detector
- Low Voltage Reset

3. PIN ASSIGNMENTS

Symbol	Descriptions	No. of Pln	Pin Count
VDDA	Power for OSC	1	1
PWMVDD	Power for PWM	2	3
VDDIO	Power for Regulator	1	4
VDDIO	Power for port1 & port3	1	5
VDDIO	Power for EA0~DA22 & ED0~ED15	2	7
VSSA	GND for OSC	1	8
PWMVSS	GND for PWM	2	10
VSSIO	GND for IO	4	14
CVDD	Power + for core	2	16
CVSS	Power - for core	1	17
VOUT	Regulator voltage output	1	18
XIN	High speed clock crystal input / RC-type oscillator input	1	19
XOUT	High speed clock crystal output / RC-type oscillator input	1	20
LXIN	Low speed clock crystal input	1	21
LXOUT	Low speed clock crystal output	1	22
CKSEL	Crystal/RC-type oscillator select for high speed clock	1	23
USBSEL	Mess storage / Vender class select pin	1	24
BP0	PPDAC output 1	1	25
BN0	PPDAC output 2	1	26
RSTB	Chip reset	1	27
TEST	For test only	1	28
EA0~EA22	Address bus of extension bus	23	51
ED0~D15	Data bus of extension bus	16	67
WR\	Write signal of extension bus	1	68
RD\	Read signal of extension bus	1	69
D+	USB Data +	1	70
D-	USB Data -	1	71
PWR+	USB power +	1	72
PWR-	USB power -	1	73
P1.0~P1.15	General I/O port P1.0~P1.15	16	89
P3.0~P3.10	General I/O port P3.0~P3.10 P3.0: INT0 pin of UART interface P3.1: INT1 pin of UART interface P3.2: INT2 / IR output P3.3: NCSB P3.4: CLE P3.5: ALE P3.6: R/B\ P3.7: WPB P3.8: CS3/EA23 P3.9: CS2 P3.10: CS1	11	100

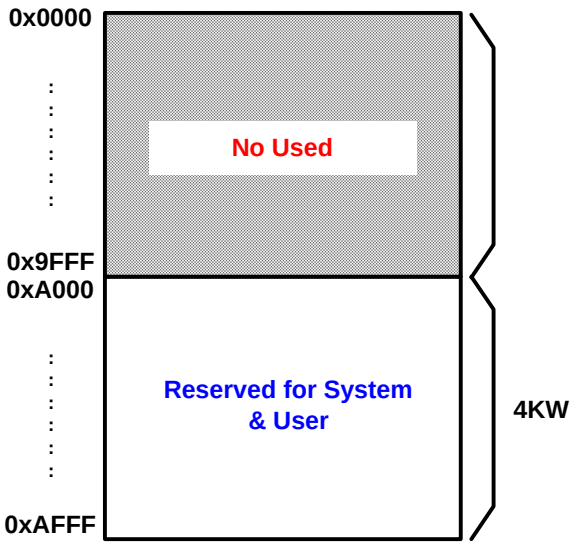
4. MEMORY

4.1 Internal ROM

SNC712 provides hi-compression algorithm to compress voice data in order to save more memory size. So all the de-compression program has be built at the internal ROM of SNC712 and system will reserved some necessary ROM space for those de-compression program automatically once user active the de-compression function. There are totally 64K words of SNC712 internal ROM, user can built-in his own program in the internal ROM for his application except necessary space for de-compression program.

4.2 Internal RAM

The internal totally 4K words RAM and the SRAM regions 0xA000~0xAFFF are reserved for system and user's application.



5. Clock System

SNC712 is a dual clock system that it provides high-speed clock (6MHz crystal up to 16MHz) and low-speed clock (32768Hz). The SNC712 use internal PLL to up sample clock speed to 16MHz.

The PLL of SNC712 is always enabling in internal circuit.

5.1 Normal Mode

The normal mode means CPU main clock source comes from 16MHZ hi-speed clock source, so SNC712 is run in full speed. There have one pin option “CKSEL”. It is hi-clock input source select pin. High is ROSC clock source input and low is 16MHz clock source input. Currently the SNC712 only support 16MHz clock source input.

5.2 Low-speed mode

This is a special operation mode of SNC712, the hi-speed clock is disabled and main clock of SNC712 comes from low-speed clock source (32768HZ). It will save much power consumption when chip works on the low-speed mode and the low-speed clock can select 32768HZ crystal for clock source.

5.3 Stop Mode

In stop mode, all the system clocks are stop (16MZH & 32768HZ) and chip entry a very low power consumption state. Chip will wake-up from stop mode once any IO state change or external interrupt occurs.

5.4 Watch Mode

This mode is for some real time clock application, users have to add a 32768HZ crystal to realize RTC function. Considering to saving power consumption, user should stop the hi-speed clock source (16MHZ) and enable the low-speed clock source. Then chip will entry power down mode but the low-speed clock still working and wake-up chip when the RTC period is happened in order to fresh the RTC timer.

There are three options for RTC interrupt periods, users can select 0.25sec/0.5sec and 1sec through the RTC control register.

If chip is in power-down mode and interrupt enable is active for RTC, then chip will be wake-up from power-down mode per 0.25/0.5/1 second.

6. POWER ON RESET

When “L” level appears on RESET PIN, the chip will enter RESET state.

After reset, the chip does not execute the first instruction until counting 2^{17} clock cycles. It takes around 8.2ms at 16MHz. (crystal for clock source), and the location of the first instruction after RESET is 0x000000. In additional, all the contents of SRAM will be unchanged during RESET stage.

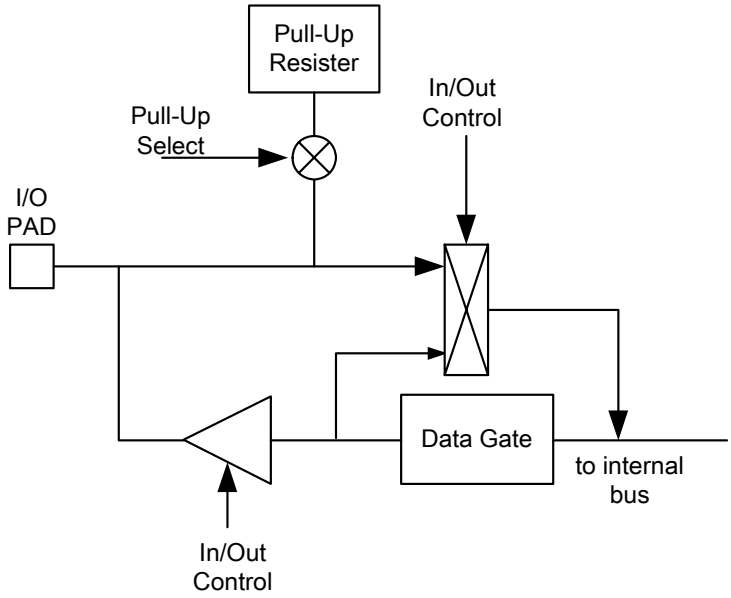
Note: All the contents of SRAM data will be set to 0x00 in Sonix standard code after reset

7. I/O PORT

SNC712 provides totally 27 I/O pins (P1.0~P1.15, P3.0~P3.10). The input pull-high resistor of each pin can be programmed by port pull-high register and the direction of I/O port is selected by port direction register. The I/O port P1.0~P1.15 can wake the chip up from the stop mode and watch mode.

These 27 programmable I/O pins provides not only a simply input/output function that also can configure to be chip select pins of extension bus. For the detail please refer to following sections.

The internal structure of I/O pins is showed in **Figure-1**.



I/O Configuration of Port1 and Port3

Figure-1

In some applications (e.g., Infra Red, IR), an output port needs to be modulated a carry signal. In the cases, the routine of modulation will occupy too many CPU computations. Thus, a modulation circuit is built in chip to reduce CPU's loading.

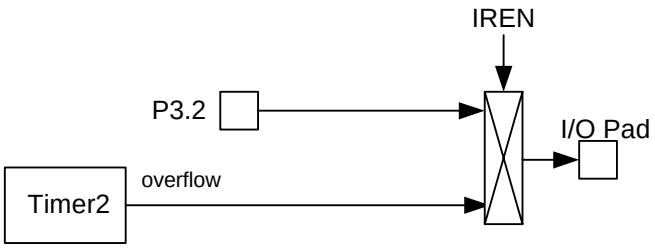


Figure-3

The modulation function will be active when the control bit “IREN” set to “1”. And setting timer2 can generate the frequency of carry signal.

8. TIMER/COUNTER

SNC712 provides three 8-bit timer/event counters (T0/T1/T2). Each timer is 8-bit binary up-count timer with pre-scalar and auto-reload function. Timer 0 (T0) was used when voice playing, so user should avoid to use T0.

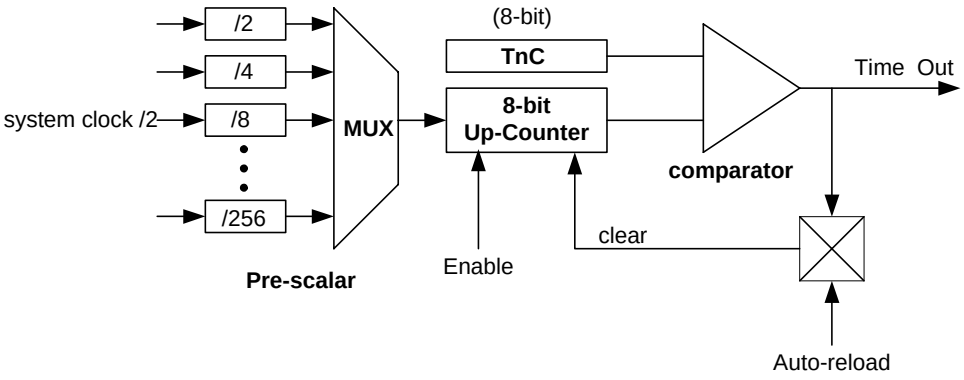


Figure-4

9. PWM Audio Output

A PWM Direct Drive circuit is built-in SNC712. The maximum resolution of PWM is 11 bits. Two huge output stage circuits are designed in SNC712. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.

10. Low Voltage Detector

SNC712 built in a low voltage detector for power management. It provides four different detect level, 2.3V, 2.5V, 2.8V and 3.1V. User can set an expect detect level through the PCR control register and polling the acknowledge bit to get the current power level is higher or lower then the detect level. Each detect level is designed by schmitt trigger architecture, that’s means each detect level has a detect window.

For example, the detect window of detect level 2.3V is 2.24V ~ 2.36V. When the VDD power down below 2.24V, the detect bit of PCR register will be set to 1. Once VDD power is recovered and must be higher then 2.36V, then detect bit is clear by system.

Detect level	Voltage window of schmitt trigger
2.3V	2.24V ~ 2.36V
2.5V	2.44V ~ 2.57V
2.8V	2.72V ~ 2.88V
3.1V	3.01V ~ 3.19V

11. EXTENSION BUS

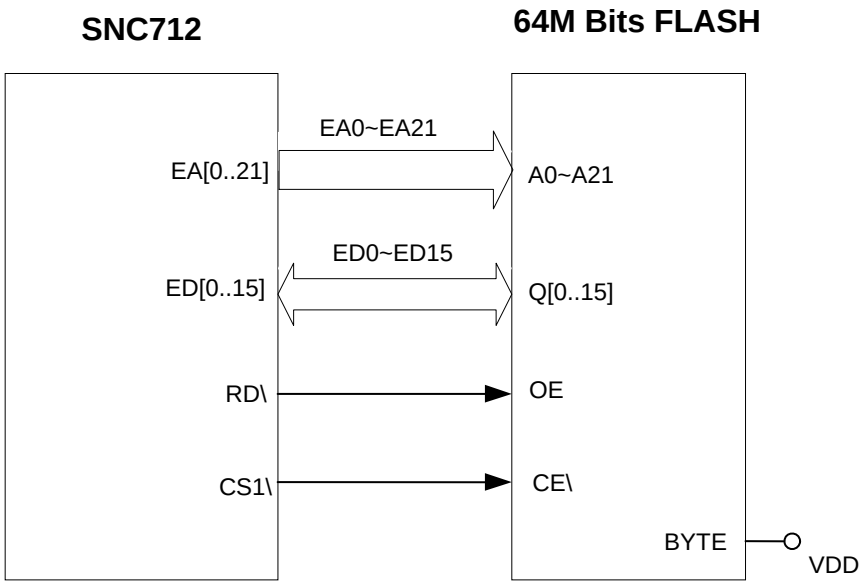
SNC712 built-in a standard 8080/6800 micro-controller interface to extends the memory capability through the extension bus. In additional, SNC712 provides word mode access bus for external memory device in order to improve the efficiency.
This extension bus also allows users to connect different external devices for his own application, such as ROM, RAM, LCM, NOR flash etc.
There are 3 chip select pins for external devices, so totally SNC712 can connect 3 different devices. The maximum addressing capability of each external device is 64M bits. User can put his program into each external memory device.

11.1 Word Mode Connection

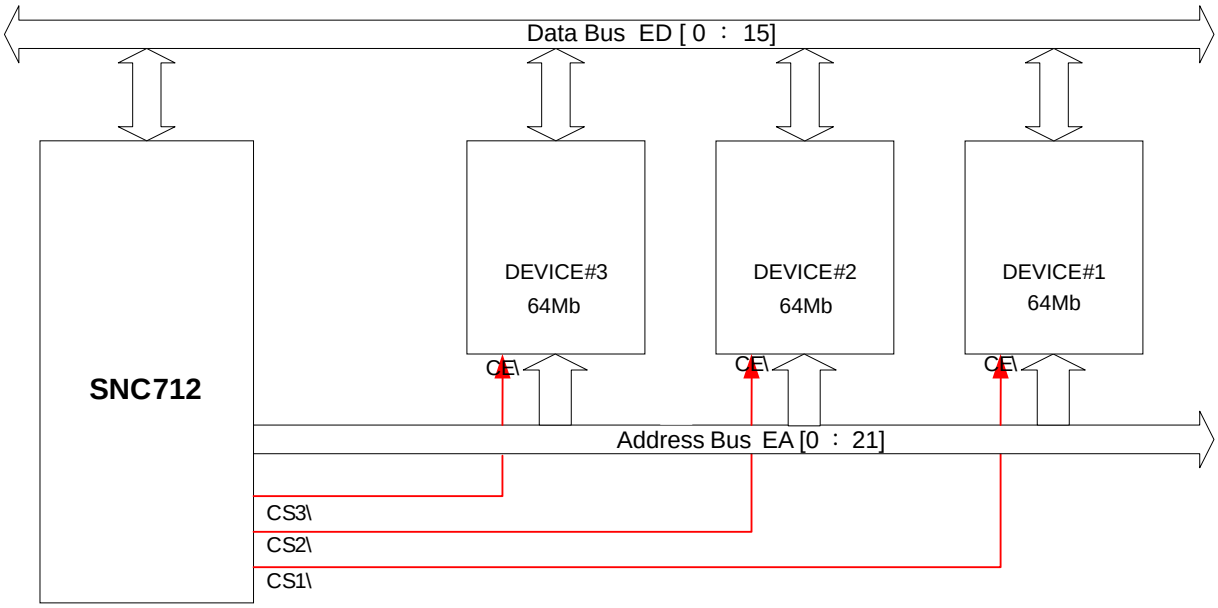
Most of hi-density memory provides word mode access. SNC712 just support word mode access bus. The connection diagram is shown as bellow. In word mode bus access, SNC712 can fetch a complete OP code or data through the 16-bit width bus at one time, and it is helpful to improved the CPU efficiency when CPU running the program from external memory device.

Device No.	Start address	End Address	Memory Size
Internal ROM	0x0000000	0x000FFFF	64K words
Reserved	0x0010000	0x01FFFFF	1984K words
Reserved	0x0200000	0x03FFFFF	2M words
1nd external device	0x0400000	0x07FFFFF	4M words
2rd external device	0x0800000	0x0BFFFFF	4M words
3th external device	0x0C00000	0x0FFFFFF	4M words

Table-1 Addressing Capability (Word Mode)



Flash Memory Word Mode Connection with 64Mb

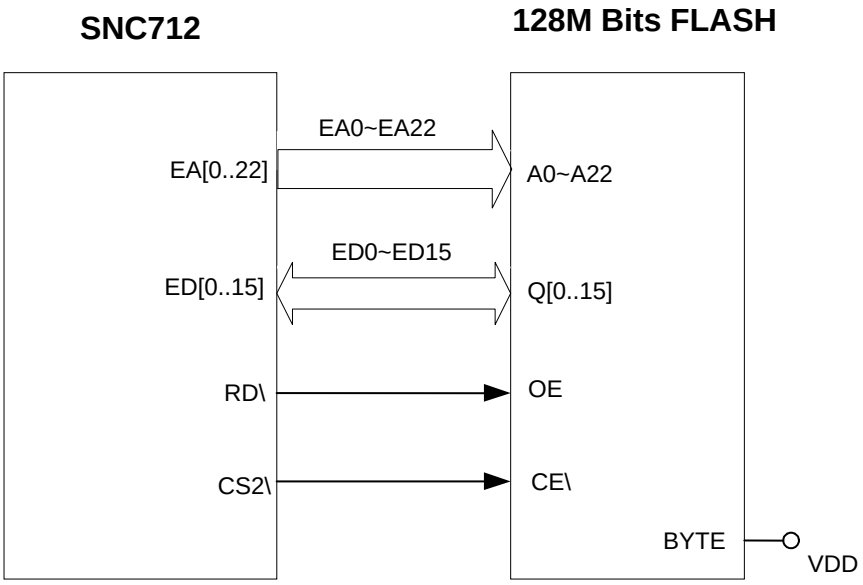


Total Support 192Mb

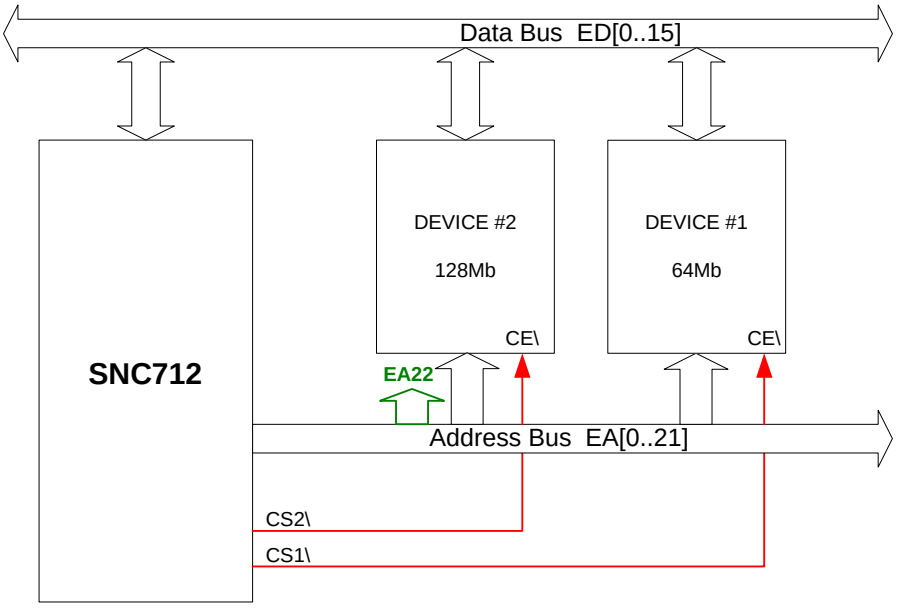
Note：In 64Mb mode, the pin EA22 is invalid.

11.2 Memory Extend

SNC712 also provides a special function that it allows to extend the addressing capability of CS2 from 64M-bit up to 128M-bit. The address pin “EA22” will as the 128M-bit address pin when user enable bit 13 of register EBCR. In additional, when bit 13 of register EBCR is enabling, the CS3 pin is invalid.



Flash Memory Word Mode Connection with 128Mb Memory



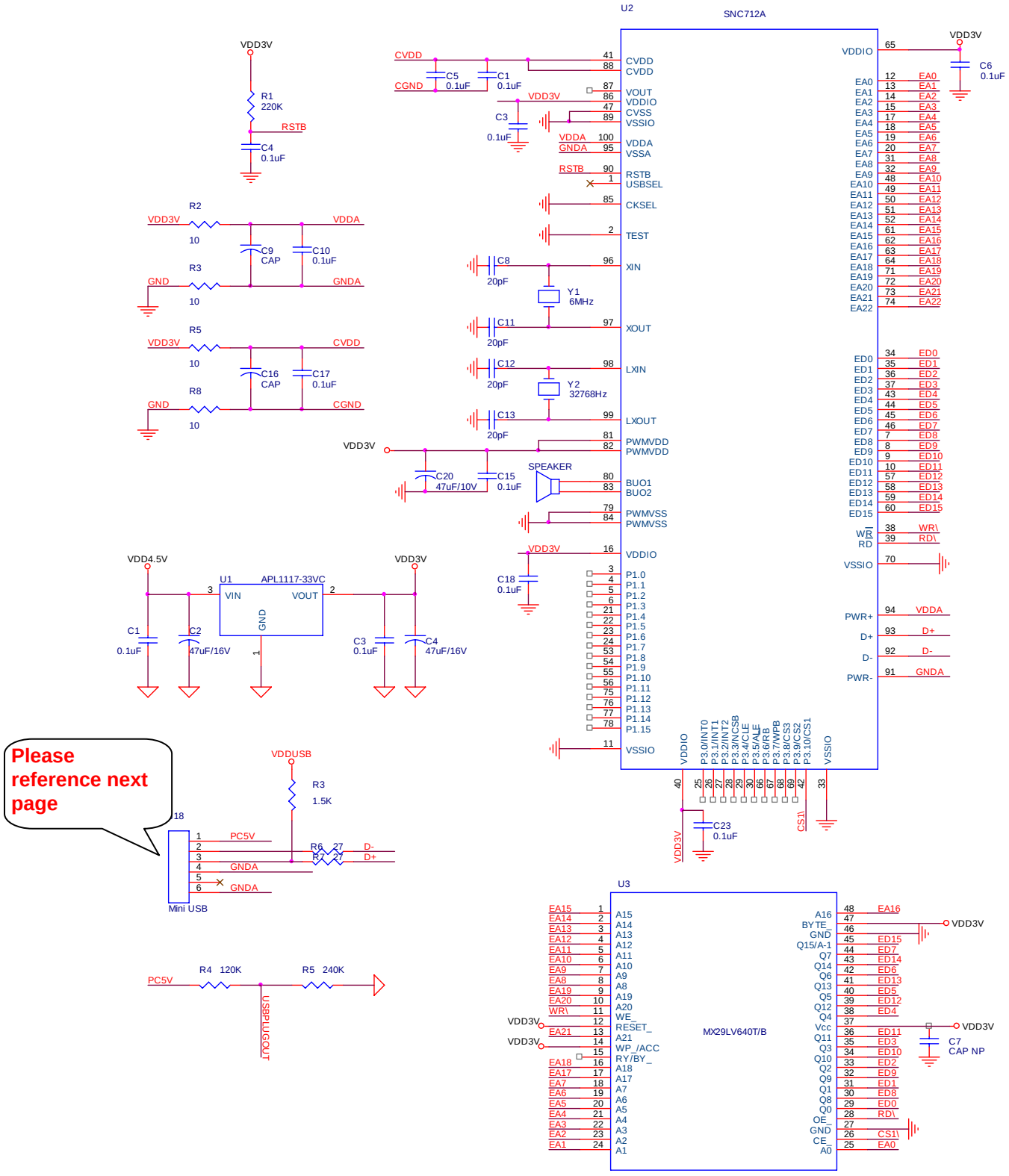
CS1 connect to 64Mb flash and CS2 connect to 128Mb flash

12. USB INTERFACE

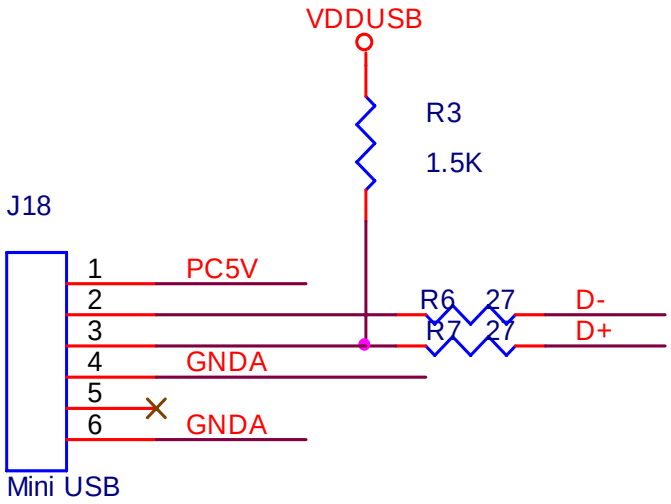
The SNC712 provides a USB 1.1 interface, user can download/upload data from/to PC through this USB interface. It supports control transfer and bulk transfer.
SNC712 provides twin buffers for data or command transition and the buffer size of those twin buffers is 64bytes.

13. APPLICATION CIRCUIT

13.1 Application circuit with USB



Mini USB Connector Description：

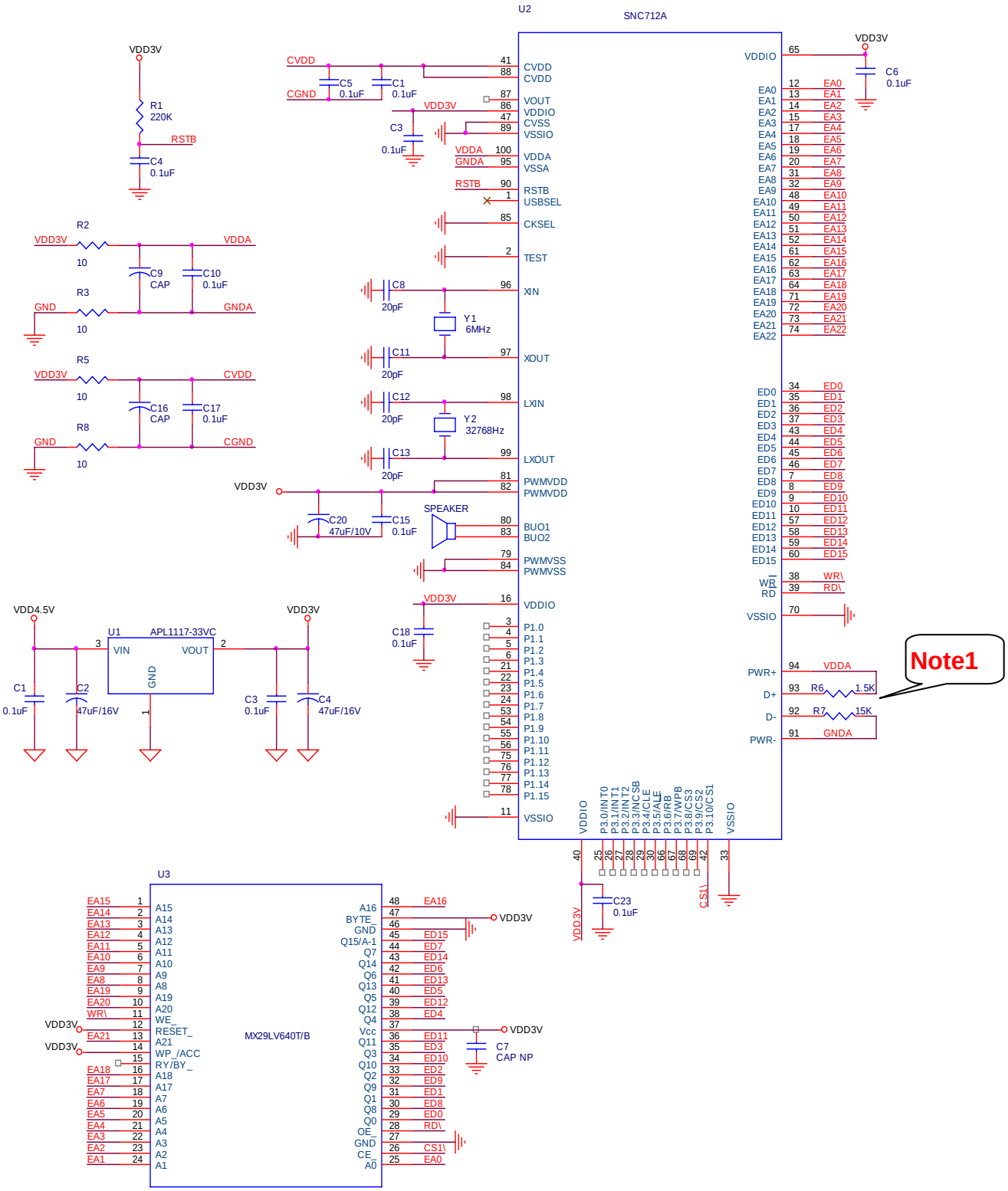


Pin No.	Description
1	VBus
2	D-
3	D+
4	ID
5	GND
6	Shell

Note1：For SNC712, please NC pin 5 of mini USB.

Note2：For SNC712, please connect shell of mini USB to analog ground.

13.2 Application circuit without USB



Note1: If user doesn't need USB function, the D+ pin and PWR+ pin must connect to 1.5K resistance to analog VDD, the D- pin and PWR- pin must connect to 15K resistance to analog ground.

14. ABSOLUTE MAXIMUM RATINGS

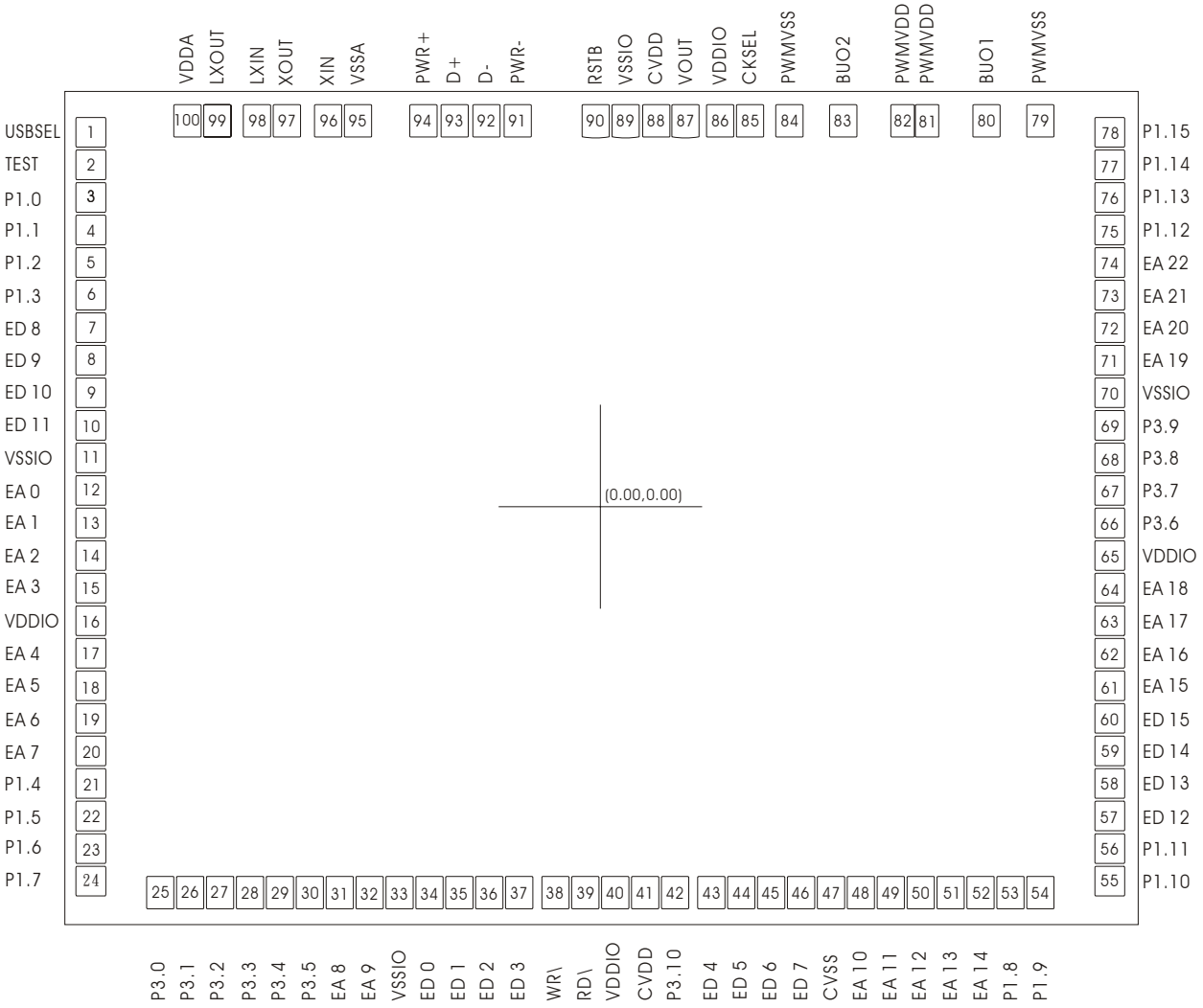
Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	6.0	V
Input Voltage	V_{IN}	GND-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55	^{o}C
Storage Temperature	T_{STG}	-55.0	125.0	^{o}C

15. ELECTRICAL CHARACTERISTICS

Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	-	3.6	V	
	V_{DD}	3.6	-	5.1	V	
Standby Current Note1	I_{SBY}	-	2.0		uA	V_{DD}=3V, no load
Operating Current	I_{OPR}	-	10		mA	V_{DD}=3V, no load
Pull-Up resistor of P1, P3.0~p3.10	R_{PU}	-	800	-	KΩ	V_{DD}=3V, no load
Input current of P1, P3	I_{IH}	-	-	10.0	uA	V_{DD}=3V,V_{IN}=3V
Input Schmitt-trigger window	-	1.5	2.5	-	V	V_{DD}=5V
Drive Current of P1, P3.0~P3.10	I_{OD}	-	4	-	mA	V_{DD}=3V,V_O=2.4V
Sink Current of P1, P3.0~P3.10	I_{OS}	-	6	-	mA	V_{DD}=3V,V_O=0.4V
Drive Current of OE, WE	I_{OD}	-	12	-	mA	V_{DD}=3V,V_O=2.4V
Sink Current of OE, WE	I_{OS}	-	10	-	mA	V_{DD}=3V,V_O=0.4V
Drive Current of Buo1	I_{OD}	360	450	-	mA	V_{DD}=3V,Buo1=1.5V
Sink Current of Buo1	I_{OS}	360	450	-	mA	V_{DD}=3V,Buo1=1.5V
Drive Current of Buo2	I_{OD}	360	450	-	mA	V_{DD}=3V,Buo2=1.5V
Sink Current of Buo2	I_{OS}	360	450	-	mA	V_{DD}=3V,Buo2=1.5V
Oscillation Freq. (crystal)	F_{OSC}	-	16	-	MHz	V_{DD}=3V
Regulator output voltage	VRO	2.6	-	2.8	V	VDD>=3.6V
Regulator supply current	IRS	-	-	20	mA	VOUT=2.6~2.8V
Reset Pin Input Schmitt-Trigger Window		1.68	-	3.81	V	VDD=5V

Note1 : Standby Current : USB Turn Off

16. BONDING PAD



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