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AMENDENT HISTORY

Version	Date	Description
Ver 1.0	May 10, 2010	First issue
Ver 1.1	May 17, 2010	Revise Serial Program I/F picture for CSP part <Section8.1.1>

1. INTRODUCTION

SNC26120P is a one-channel voice synthesizer One Time Program IC with PWM direct drive circuit. It built in a 4-bit tiny controller with one 4-bit input port and two 4-bit I/O ports. By programming through the tiny controller in SNC26120P, user's varied applications including voice section combination, key trigger arrangement, output control, and other logic functions can be easily implemented.

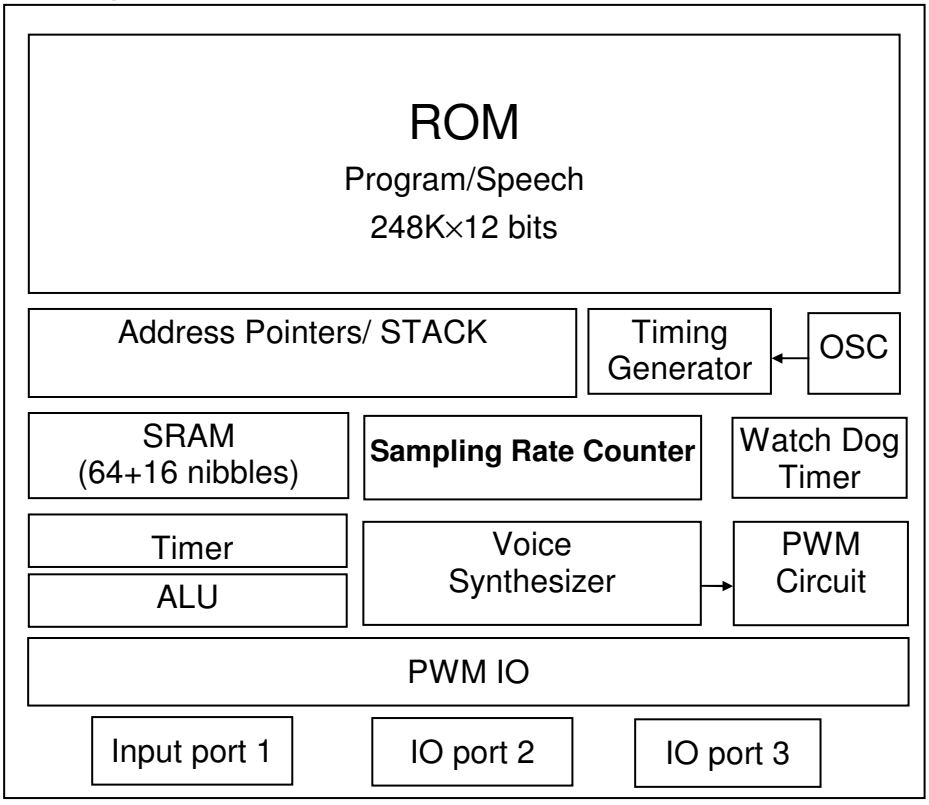
2. FEATURES

- Single power supply 2.4V – 5.5V
- 120 seconds voice capacity are provided (@6KHZ sample rate)
- Built in a 4-bit tiny controller
- I/O Port
  - One 4-bit Input port P1is provided.
  - Two 4-bit I/O ports P2 and P3 are provided.
  - The driving/sink current of P2 & P3 is up to 8mA/16mA
  - The IO pins P2.3 can be modulated with 38.5Khz carry signal to implement IR function.
  - PWM output for IO (P2.0~P2.3, P3.0~P3.3)
- (64+16)*4 bits RAM are provided.
  (Notes : m0~m63 + 16 PWMIO duty registers)
- Maximum 64k program ROM is provided
- 248K*12 shared ROM for voice data and program
- Readable ROM code data
- Voice Synthesizer:
  - Single channel speech output.
  - Support 4-bits SONiX-ASDPCM and 8-bit PCM algorithm
- Adaptive playing speed from 2.5k-20kHz is provided
- Built in an PWM circuit output, can directly connected to Speaker for sound output.
- System clock: 2MHz
- Event Mark function supported
- Low Power Detect.
- Watch Dog Timer Supported

3. PIN ASSIGNMENT

Symbol	I/O	Function Description
P10~P13	I	Input port 1
P20~P23	I/O	I/O port 2: IO
P30~P33	I/O	I/O port 3: IO
Rosc	I	Oscillation component connection pin
BUO1	O	PWM output 1
BUO2	O	PWM output 2
RST	I	RST=1→ Reset Chip (Active H)
CVDD	I	Positive power supply for CPU
CGND	I	Negative power supply for CPU
VDDIO	I	Positive power supply for I/O
GNDIO	I	Negative power supply for I/O
RVIN	I	Regulator VIN
RVOUT	O	Regulator VOUT
RGND	I	Regulator GND
Test	I	Test pin
VPP0	I	OTP Programming Voltage
VPP1	I	OTP Programming Voltage
VPP2	I	OTP Programming Voltage
CSP	I	Chip Select Pin (0: 26120P <Default>)

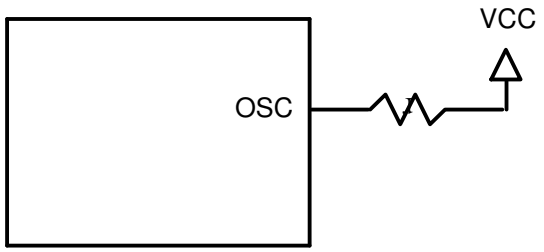
4. Block Diagram



5. FUNCTION DESCRIPTIONS

5.1 Oscillator

SNC26120P accepts RC type oscillator for system clock. The typical circuit diagram for oscillator is listed as follows.



RC Oscillator

5.2 ROM

SNC26120P contains a substantial 248K words (12-bit) internal ROM, which is shared by program and resource data. Program, voice and data are shared within this same 248K words ROM.

5.3 RAM

SNC26120P contains (64+16) nibble RAM <(64+16) x 4-bits>. The 64 nibble RAM is only one page. Another 16 nibbles are 16 PWMIO duty registers. In our programming structure, user can Directly use memory related command, M0 ~ M63 in the data transfer type instructions, to access first 64 nibbles. Another 16 nibbles, user can use PWMxL, PWMxH related command to access when PWMIO function is disabled. (x can be 1~8)

5.4 Power Down Mode

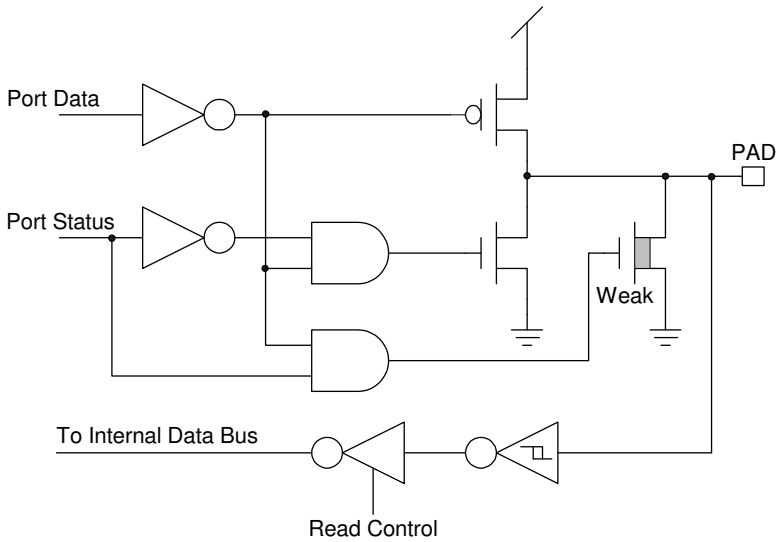
"End" instruction makes the IC entering into Stop Mode will stop the system clock for power savings. Any valid data transition (L→H or H→L) occurring on any IO pin can be used to start the system clock and return to normal operating mode.

5.5 Sampling Rate Counter

The unique sampling rate counter is designed in voice channel to be able to play diverse voices at different sample playing rates. The playing rate can be adaptively set up among from the wide ranges of 2.5KHz to 20KHz. This architecture yields a high-quality voice synthesis that sounds very close to its original source when played through the same amplifier and speaker circuitry.

5.6 I/O Ports

There are one 4-bit input port P1 and two 4-bit I/O ports P2 and P3. Any I/O can be individually programmed as either input pull low or output. Any valid data transition (H→L | L→H) of P1,P2 and P3 can reactivate the chip when it is in power-down stage.



I/O Port Configuration

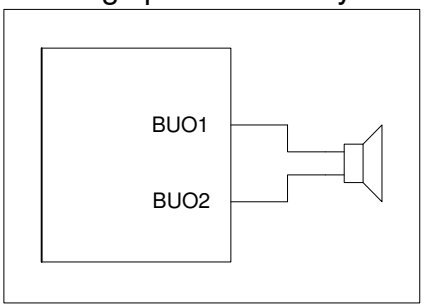
Note:

(1) ***Weak N-MOS can serve as pull-low resistor.***

(2) ***The driving/sink current of P2 & P3 is up to 8mA/16mA***

5.7 PWM Output

An PWM circuit is built-in SNC26120P. The maximum resolution of PWM is 8 bits. Two huge output stage circuits are designed in SNC26120P. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.



PWM Output

5.8 Watch Dog Timer

SNC26120P built an internal WDT (Watch Dog Timer). This Watchdog timer would issue resets signal to this chip if it is not cleared before reaching terminal count (128 ms). The watchdog timer is enabled at reset and cannot be disabled.

5.9 IR Function

P23 can be modulated with 38.5KHz square wave before sent out to P23 pin.
The IR signal can be achieved by this modulated signal.

5.10 PWM IO control

SNC26120P has support 8 PWM IO (P20~P23, P30~P33). Each I/O has 8 bit independent duty register, and the 8 bit register are compare with 8 bits counter. If set use PWM IO function and internal counter start at 000H, the mapping I/O will set High. The 8 bits counter increment if the same duty register, that will reset the mapping IO pin.

6. ABSOLUTE MAXIMUM RATING

Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55.0	°C
Storage Temperature	T_{STG}	-55.0	125.0	°C

7. ELECTRICAL CHARACTERISTICS

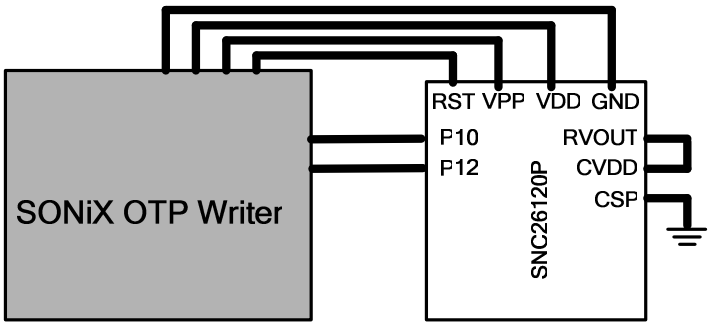
Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.0	5.5	V	
Program Mode Voltage (OTP)	VPP	7.25	7.5	7.75	V	OTP Programming Voltage In Normal Mode Vpp can be floating.
Standby current*	I_{SBY}	-	5	-	*u*A	V_{DD}=3V, no load
Operating Current*	I_{OPR}	-	5	-	mA	V_{DD}=3V, no load
Input current of P1, P2, P3	I_{IH}	-	3.0	-	*u*A	V_{DD}=3V,V_{IN}=3V
Drive current of P2, P3	I_{OD}	6	8	-	*m*A	V_{DD}=3V,V_O=2.4V
Sink current of P2, P3	I_{OS}	10	16	-	*m*A	V_{DD}=3V,V_O=2.4V
PWM current	I_{PWM}	-	300	-	*m*A	VDD=3V, BUOx=1.5V
Oscillation Freq.	F_{OSC}	1.98	2.05	2.12	MHz	V_{DD}=3V, Temp.=25°C @Rosc = 220 Kohm Min : -3% Max : +3%

* Notes : Include SNC26120 Core IC + OTP

8. APPLICATION CIRCUIT

8.1 I/F of Programming mode

8.1.1. Serial Program I/F.



If user would like to program BIN file into OTP by SONIX OTP Writer V1.0 with **serial programming** way. There are total **6** pins programming pins are necessary.

Also, there are some points for serial program

(1) VPP should connect to VPP0/VPP1/VPP2

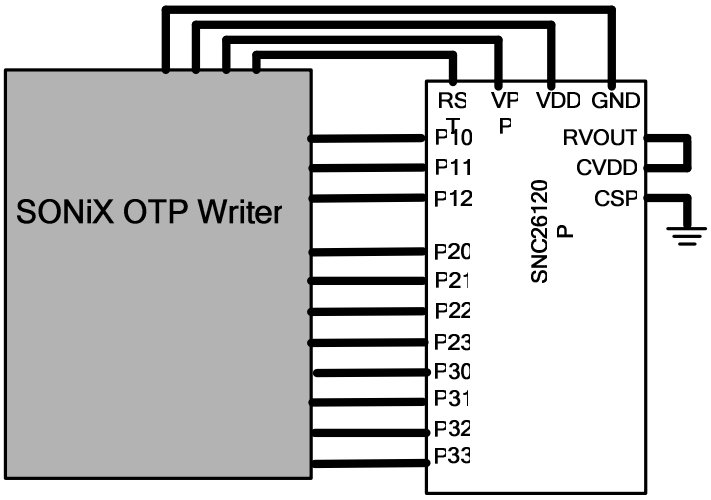
(2) VDD should connect to VDDIO/RVIN

(3) RVOUT/CVDD should short together

(4) GND should connect to GNDIO/CGND/ RGND

(5) CSP should be floating or connect to GND on user's PCB.

8.1.2. Parallel Program I/F



If user would like to program BIN file into OTP by SONIX OTP Writer V1.0 with **parallel programming** way. There are total **15** pins programming pins are necessary.

Also, there are some points for parallel program

(1) VPP should connect to VPP0/VPP1/VPP2

(2) VDD should connect to VDDIO/RVIN

(3) RVOUT/CVDD should short together

(4) GND should connect to GNDIO/CGND/ RGND

(5) CSP should be floating or connect to GND on user's PCB.

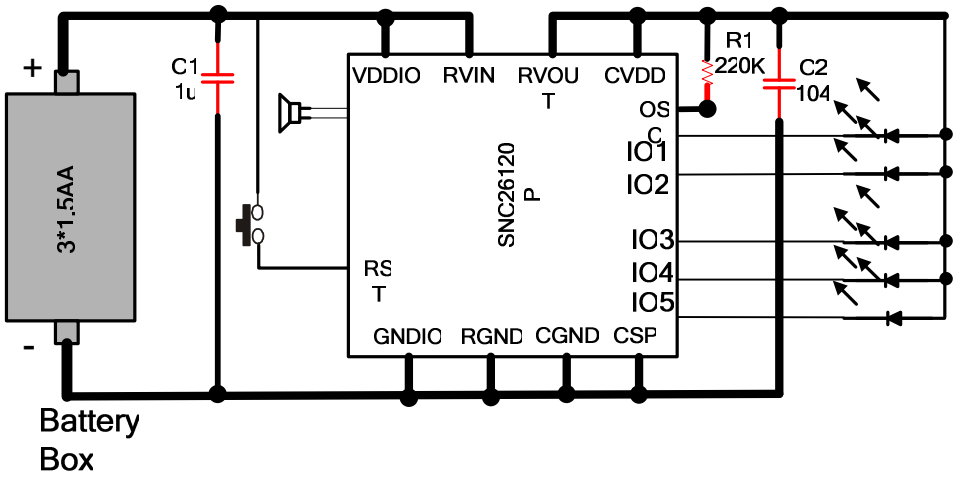
8.2 General application

8.2.1.In 5V application :

(1) CSP should be floating or connect to GND (CSP=0 : SNC26120P)

(2) VDDIO/RVIN short together and connect to source power

(3) RVOUT/CVDD short together, but not connect to VDDIO/RVIN/source power.

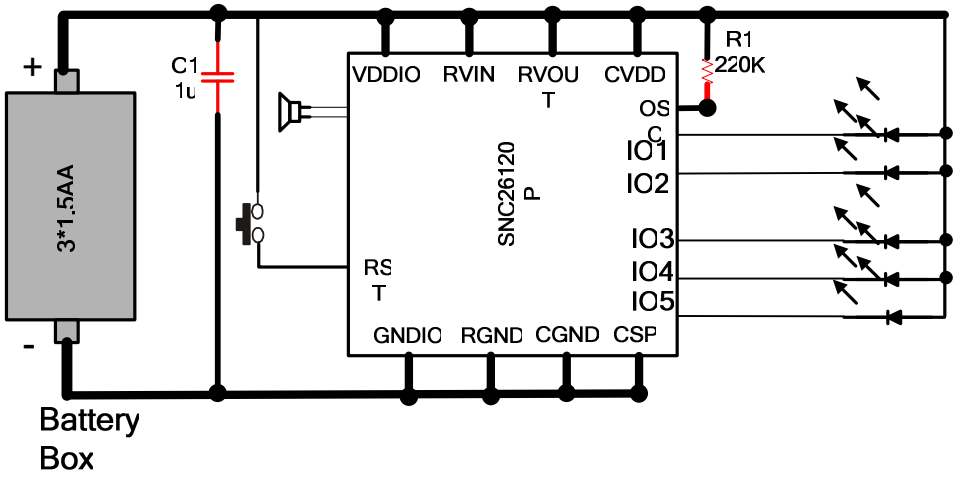


It is suggested to add a capacitor (C1 and C2), 1u and 104, it will keep power stable with general application. And this capacitor is strongly suggested to be as close to the chip as possible.

8.2.2. In 3V application :

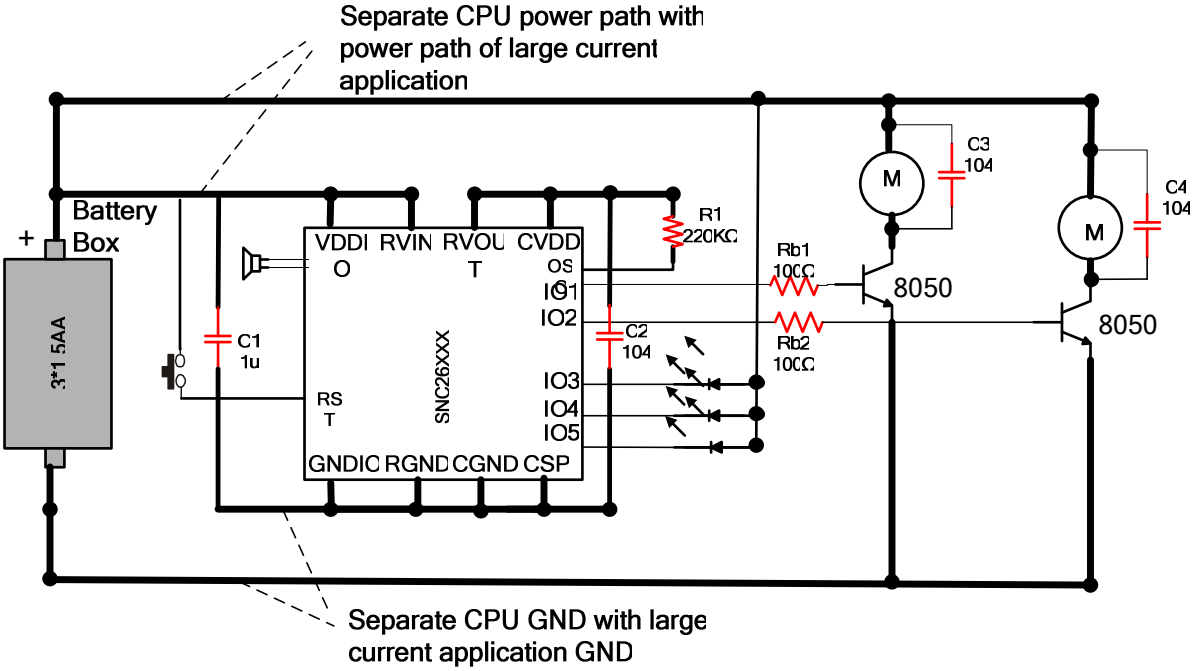
(1) CSP should be floating or connect to GND (CSP=0 : SNC26120P)

(2) VDDIO/RVIN/RVOUT/CVDD short together and connect to source power



It is suggested to add a capacitor (C1), 1u , it will keep power stable with general application. And this capacitor is strongly suggested to be as close to the chip as possible.

8.3 Motor application



There are some suggestions about PCB layout when user use SNC26120P IC with motor applications.

(1) The capacitor C1 (1u) C2 (104) is strongly suggested to be as close to the chip as possible.
(2) It had better let OSC components (R) get close to IC chip.

(3) OSC components had better get far away large current applications.

(4) Separate IC power path with large current application power path to avoid affect IC working by power drop from large current application.

(5) Let power cable thicker, especially for large current application.

(6) C3 and C4 (104) are connected at the positive point and negative point of the motor.

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