========== CONTENTS ==========

AMENDENT HISTORY

Version	Date	Description
Ver1.0	November 08, 2006	First issue
Ver1.1	April 04,2007	1. Oscialltor only support external R 2. Application circuit, if have bonding option to ground, must connect resistance between IO and Ground
Ver1.2	May 7, 2007	1. Revise 8.application circuit, remove about bonding option mode the resistor between IO and Ground.
Ver1.3	May 11,2007	1. Revise 8.application circuit (added ext. Rosc & current DAC)
Ver1.4	May 16, 2007	1. Revise 3. Pin assignment 2. Revise 5.11 Push-Pull DAC & Current DA Output. (revise Push-Pull DAC output description) 3. Revise 8. Application circuit (added P6).

1. INTRODUCTION

SNC21300 is a one-channel voice synthesizer IC with Push-Pull direct drive circuit. It built-in a 4-bit tiny controller with four 4-bit I/O ports. By programming through the tiny controller in SNC21300, user's varied applications including voice section combination, key trigger arrangement, output control, and other logic functions can be easily implemented.

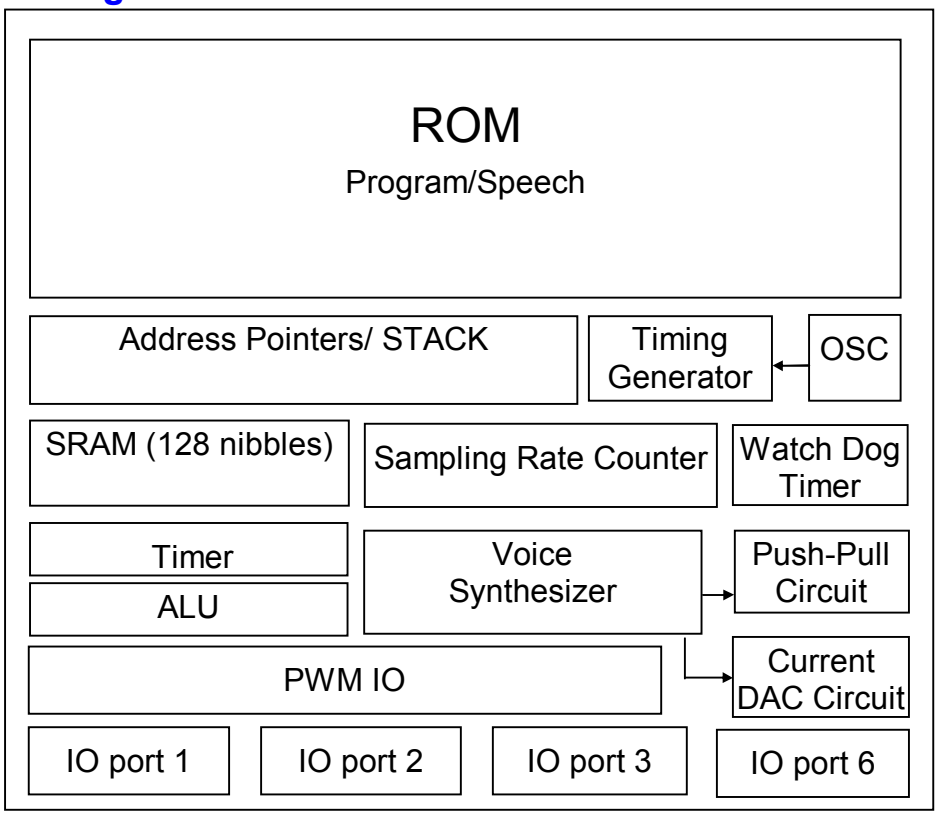
2. FEATURES

- Single power supply 2.4V – 5.5V
- System Clock is 2MHz, the instruction cycle is 4us
- 300 seconds voice capacity are provided (@6KHZ sample rate)
- Built in a 4-bit tiny controller
- I/O Port
  - Four 4-bit I/O ports P1, P2, P3 and P6 are provided
  - The driving/sink current of P3.2 & P3.3 is up to 8mA/16mA
  - The IO pins P3.3 or P2.3 can be modulated with 38.5Khz carry signal to implement IR function.
  - PWM output for IO (P3.0~P3.3)
- 128*4 bits RAM are provided
- Maximum 16k program ROM is provided
- 912K*10 shared ROM for voice data and program
- Readable ROM code data
- Built-in one channel High Quality speech synthesizer
- Adaptive playing speed from 2.5k-20kHz is provided
- Automatic repetition
- Support 5-bit ADPCM and 10 bit PCM format
- Built in an 8-level volume control Push-Pull DAC circuit output, can directly connected to Speaker for sound output
- 12 bit Push-Pull DA output and 12 bit current DAC output
- Event Mark function supported
- Low-Voltage Detect circuit
- Watch Dog Timer Reset function.

3. PIN ASSIGNMENT

Symbol	I/O	Function Description
P10~P13	I/O	I/O port 1: IO
P20~P23	I/O	I/O port 2: IO
P30~P33	I/O	I/O port 3: IO
P60~P63	I/O	I/O port 6: IO
RST	I	Reset Chip (Active H)
TEST1	I	Test Pin
TEST2	I	Test Pin
OSC	I	Oscillation component connection pin
DAON	O	Push-Pull output 1
DAOP	O	Push-Pull output 2
DACO	O	Current DAC output
VDD	P	Positive power supply
GND	P	Negative power supply

4. Block Diagram



5. FUNCTION DESCRIPTIONS

5.1 Oscillator

System clock define 2MHz, the source provided by external resistor ring oscillator.

5.2 ROM

SNC21300 contains a substantial maximum 912K words (10-bit) internal ROM, which is shared by program and resource data. Program, voice and data are shared within this same 912K words ROM.

5.3 RAM

SNC21300 contains maximum 128 nibble RAM (128 x 4-bits). The 128 nibble RAM is divided into eight pages (page 0 to page 7, 16 nibble RAM on each page). In our programming structure, users can use the instructions, PAGE n (n=0 to 7) to switch and indicate the RAM page. Besides, users can use direct mode, M0 ~ M15 in the data transfer type instructions, to access all 16 nibbles of each page.

5.4 Power Down Mode

"End" instruction makes the IC entering into Stop Mode will stop the system clock for power savings (<3uA @VDD=3V and <6uA @VDD=4.5V.) Any valid data transition (L à H or H à L) occurring on any IO pin can be used to start the system clock and return to normal operating mode.

5.5 Sampling Rate Counter

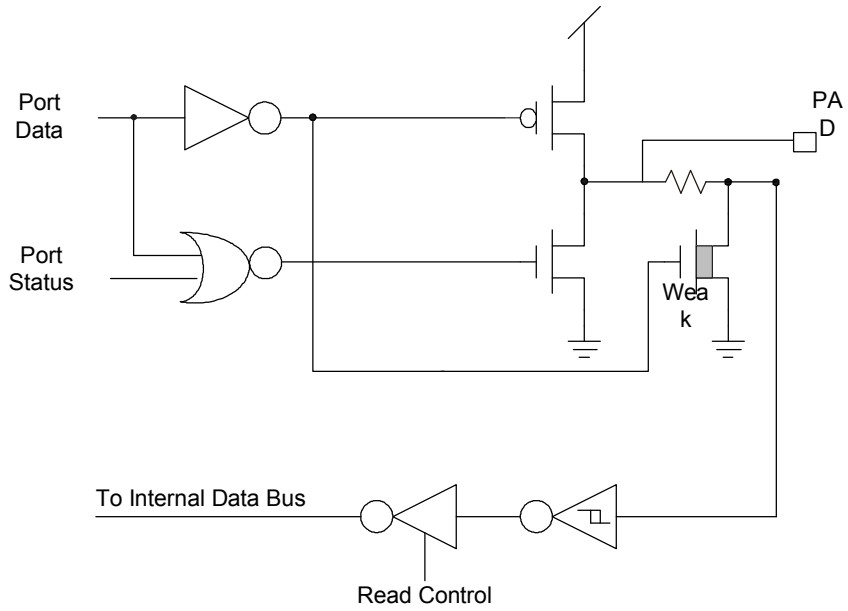
The unique sampling rate counter is designed in voice channel to be able to play diverse voices at different sample playing rates. The playing rate can be adaptively set up among from the wide ranges of 2.5KHz to 20KHz. This architecture yields a high-quality voice synthesis that sounds very close to its original source when played through the same amplifier and speaker circuitry.

5.6 Auto Repeat Function

A voice section can be repeated by the built-in special hardware of SNC21300 without any software effort. The function activated by setting the corresponding bit of a control register. Once the control register was setting, the channel will continue to play the voice section (the Next Section).

5.7 I/O Ports

There are four 4-bit I/O ports P1, P2, P3 and P6. Any I/O can be individually programmed as either input pull low or output. Any valid data transition (H à L or L à H) of P1, P2, P3 and P6 can reactivate the chip when it is in power-down stage.



I/O Port Configuration

Note:

(1) ***Weak N-MOS can serve as pull-low resistor.***

(2) ***The driving/sink current of P3.3 & P3.2 is up to 8mA/16mA***

5.8 IR Function

Bit 3 of Mode Register is applied to control the IR function. P33 can be modulated with 38.5KHz square wave before sent out to P3.3 or P2.3 pin. P3.3 and P2.3 out is controlled by Mode1.1. If Mode1.1 set 1 IR is use P2.3, set “0” is use P3.3. The IR signal can be achieved by this modulated signal.

5.9 PWM IO control

SNC21300 has support 4 PWM IO (P30~P33). Each I/O has 8 bit independent duty register, and the 8 bit register are compare with 8 bits counter. If set use PWM IO function and internal counter start at 000H, the mapping I/O will set High. The 8 bits counter increment if the same duty-register, that will reset the mapping IO pin.

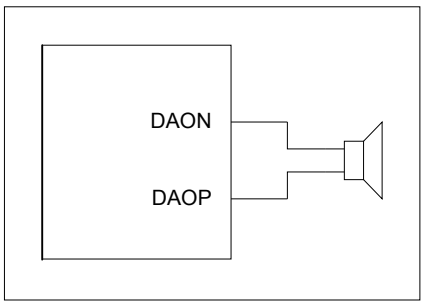
5.10 Watch Dog Timer

SNC21300 built-in an internal WDT (Watch Dog Timer). This Watchdog timer would issue resets signal to this chip if it is not cleared before reaching terminal count (1 sec). The watchdog timer is enabled at reset and cannot be disabled.

5.11 Push-Pull DAC & Current DA Output

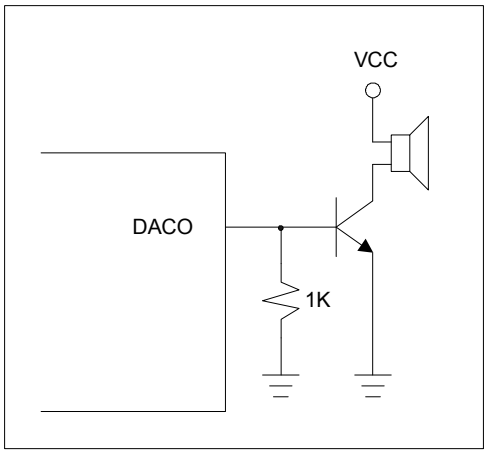
SNC21300 is an advanced chip to be designed having two optimal methods to play out the voices. One is DAC and the other is Push-Pull DAC. Upon user's applications, user can select either DAC or Push-Pull DAC in his design. Please be aware that only one method can be activated at the time.

Push-Pull DAC: An 8-level volume control Push-Pull DAC circuit is built-in SNC21300. The maximum resolution of Push-Pull DAC is 12 bits. Two huge output stage circuits are designed in SNC21300. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.



Push-Pull DAC Output

DAC: A 12-bit current type digital-to-analog converter is built-in SNC21300



DAC Output

5.12 Event Mark

This is a new function for SNC21300 series, it allows user to add a special mark in wave data by the voice edit tool "CoolEdit", "Goldwav", "SoundForge". User can insert event tags in anywhere of his wave file and can easy to get this special code to do his special action during voice playing. That means, it should be easily to control the I/O (such as LED or Motor) and other actions to synchronize with voice.

6. ABSOLUTE MAXIMUM RATING

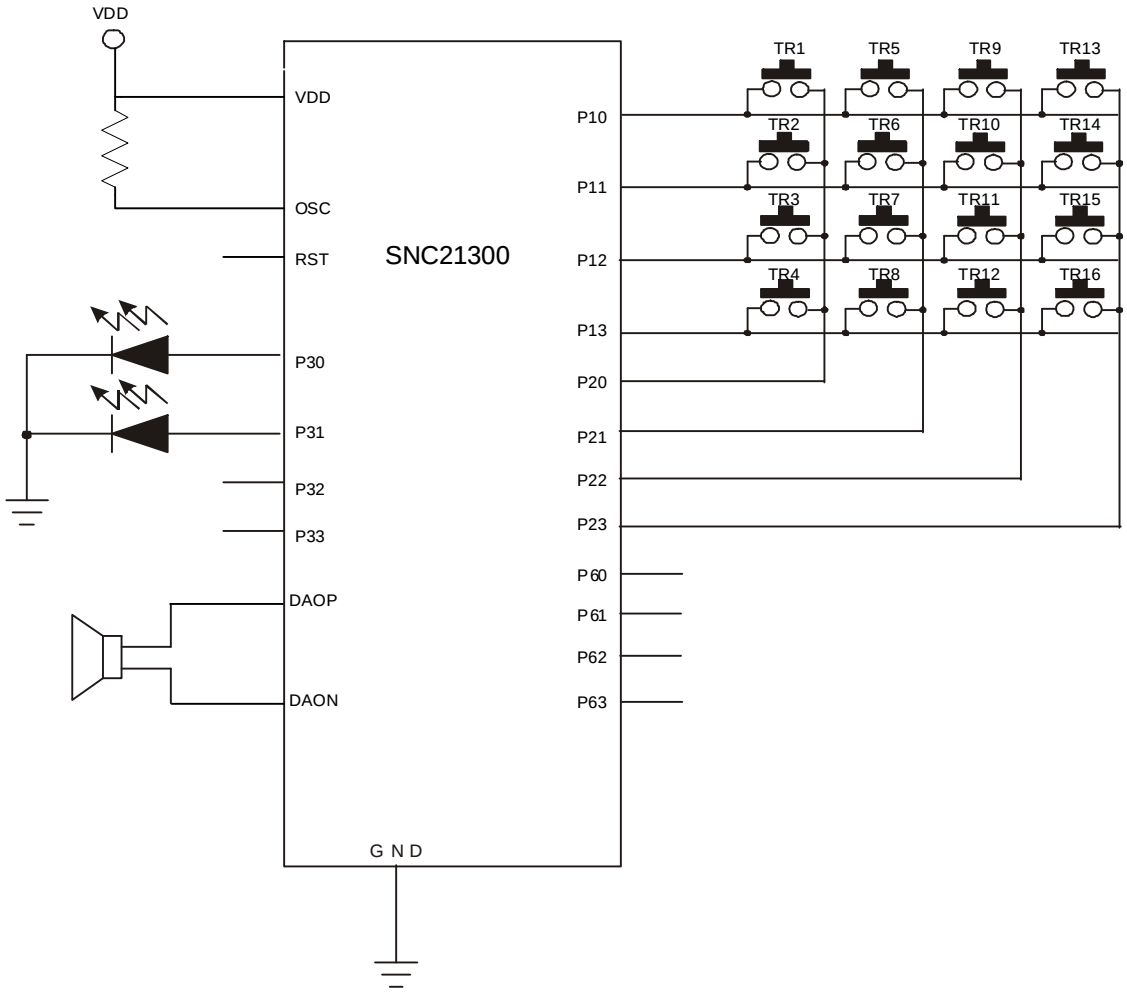
Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55.0	°C
Storage Temperature	T_{STG}	-55.0	125.0	°C

7. ELECTRICAL CHARACTERISTICS

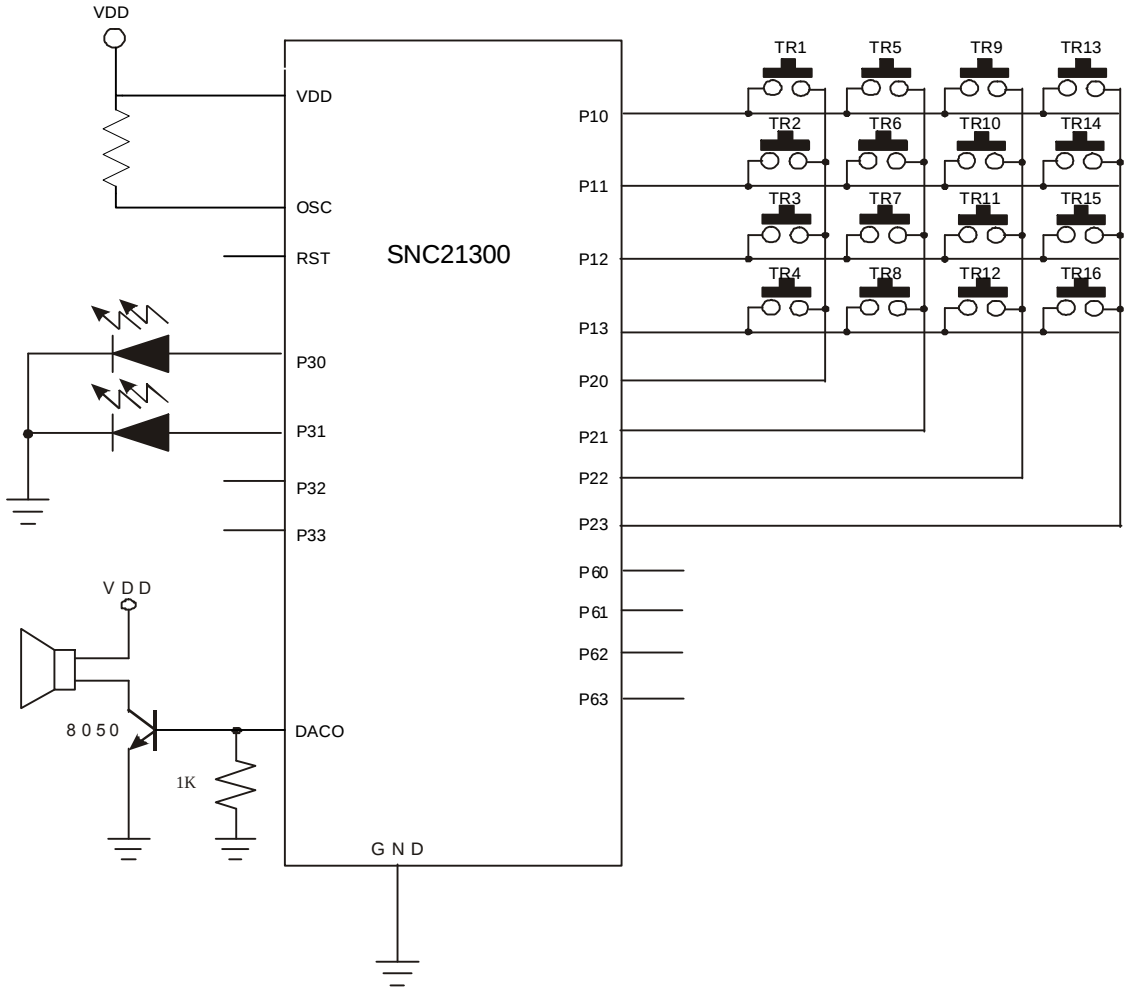
Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.0	5.5	V	
Standby current	I_{SBY}	-	3.0 5.0	-	*u*A	V_{DD}=3V, no load V_{DD}=4.5V, no load
Operating Current	I_{OPR}	-	300	-	*u*A	V_{DD}=3V, no load
Input current of P1, P2, P3, P6	I_{IH}	-	3.0	-	*u*A	V_{DD}=3V,V_{IN}=3V
Drive current of P1, P2, P3.0, P3.1, P6	I_{OD}	3	4	-	*m*A	V_{DD}=3V,V_O=2.4V
Sink Current of P1, P2, P3.0, P3.1, P6	I_{OS}	4	6	-	*m*A	V_{DD}=3V,V_O=0.4V
Drive current of P3.2, P3.3	I_{OD}	6	8	-	*m*A	V_{DD}=3V,V_O=2.4V
Sink current of P3.2, P3.3	I_{OS}	10	16	-	*m*A	V_{DD}=3V,V_O=2.4V
Push-Pull DAC current	I_{PP}	-	70	-	*m*A	VDD=3V, Output 1K Sin wave.
Push-Pull DAC current	I_{PP}	-	100	-	*m*A	VDD=4.5V, Ouput 1K Sin wave.
Drive Current of DACO	I_{OD}		3		*m*A	VDD=3V,DACO=0.7V
Oscillation Freq.	F_{OSC}	-	2.0	-	MHz	V_{DD}=3V

8. APPLICATION CIRCUIT

8.1 Push-Pull DAC output Application Circuit



8.2 Current DAC output Application Circuit



DISCLAIMER

The information appearing in SONiX web pages (“this publication”) is believed to be accurate.

However, this publication could contain technical inaccuracies or typographical errors.

The reader should not assume that this publication is error-free or that it will be suitable for any particular purpose. SONiX makes no warranty, express, statutory implied or by description in this publication or other documents which are referenced by or linked to this publication. In no event shall SONiX be liable for any special, incidental, indirect or consequential damages of any kind, or any damages whatsoever, including, without limitation, those resulting from loss of use, data or profits, whether or not advised of the possibility of damage, and on any theory of liability, arising out of or in connection with the use or performance of this publication or other documents which are referenced by or linked to this publication.

This publication was developed for products offered in Taiwan. SONiX may not offer the products discussed in this document in other countries. Information is subject to change without notice. Please contact SONiX or its local representative for information on offerings available. Integrated circuits sold by SONiX are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only.

The application circuits illustrated in this document are for reference purposes only. SONIX DISCLAIMS ALL WARRANTIES, INCLUDING THE WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. SONIX reserves the right to halt production or alter the specifications and prices, and discontinue marketing the Products listed at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders.

Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by SONIX for such application.